

# Compal Confidential

## Schematics Document

### AUBURNDALE/CLARKSFIELD with Intel IBEX PEAK-M core logic Versace

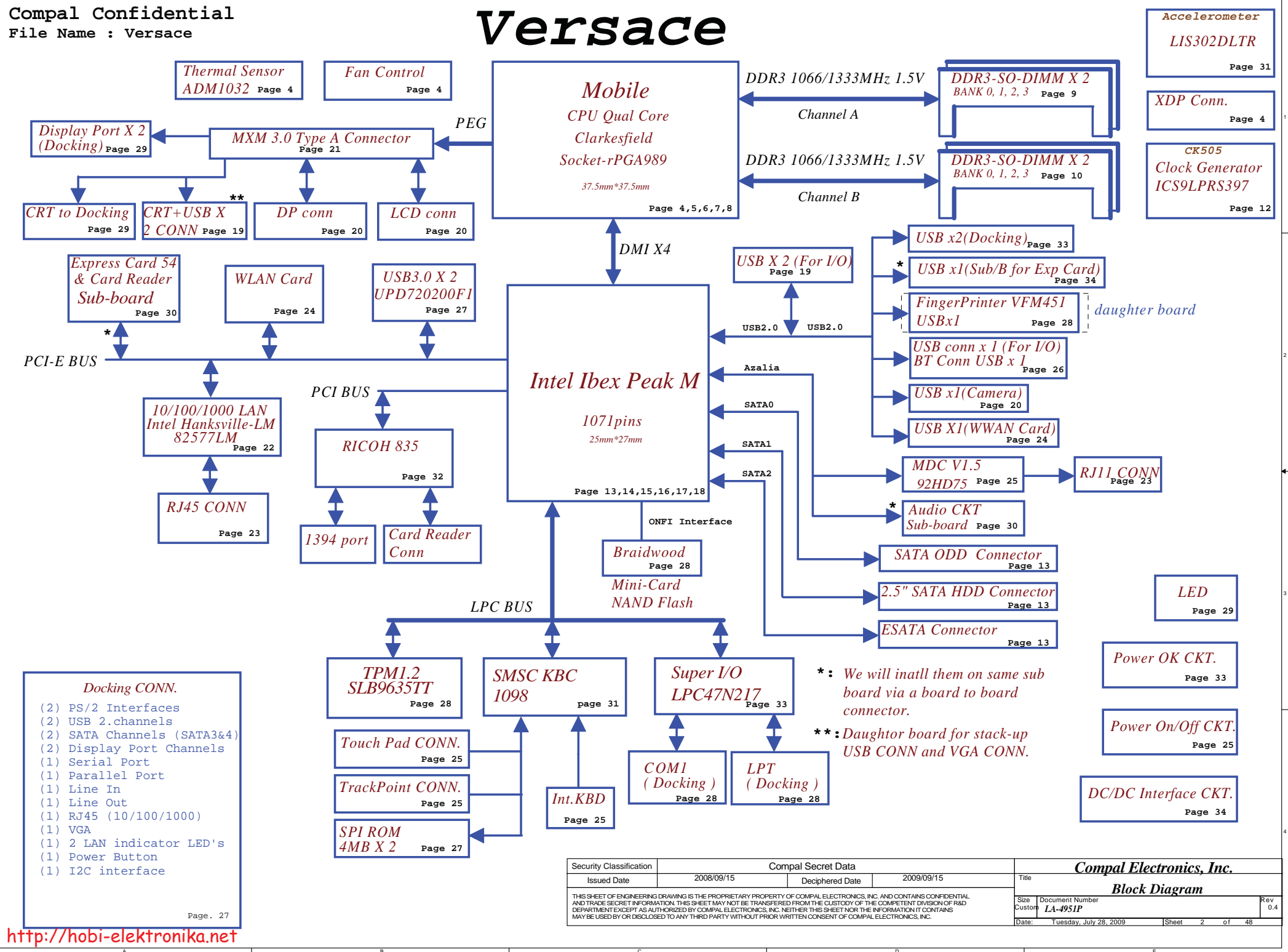
2009-07-24

REV:0.4



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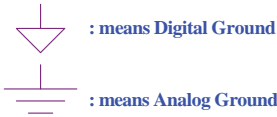
# Versace



Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.1

- DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*
- M92@ : Install for M92 Graphic controller
- 8072@ : Install for 8072 NIC controller
- 1098@ : Install for 1098 KBC controller
- CK32@ : Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

- 45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

- @ : means just reserve , no build
- CONN@ : means ME part.
- M93@ : Install for M93 Graphic controller
- 8075@ : Install for 8075 NIC controller
- 1091@ : Install for 1091 KBC controller
- CK72@ : Install for 72 pin CLOCK GEN

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DAI	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	X
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

Layout note:

1. Place C1 & C408 close to U1 pin.
2. Place U1 close to JCFAN1.

Change R5 to 220hm from 680hm. 11/30

U1 SMC2113-2-AX OFN16 4X4

Add C408. 11/30

6.8K to setup Q1 E-diode1. 12/04

U1 SMC2113-2-AX OFN16 4X4

16 REMOTE2+ 15 REMOTE2- 14 R9 2200P\_0402\_50V7K 2 2.05K\_0402\_1% C408

13 R10 1 2 6.8K\_0402\_5% 3VS

12 GND

11 FAN\_PWM\_OUT R133 10K\_0402\_5% 2 3VS

10 TACH

9 SMB\_CLK\_S3 9,10,12,14,26

8 SMDATA

7 SYS\_SHDN#

6 ALERT#

5 ADDR\_SEL

4 PWM\_IN

3 VDD

2 DP

1 DN

H\_THERMDC

H\_THERMDA C1 2200P\_0402\_50V7K

R35 1 2 10K\_0402\_5% FAN\_PWM

31 FAN\_PWM

R13 1 2 10K\_0402\_5%

3VS THER

16,21 THERM\_SCIF

R18 1 2 10K\_0402\_5% @10K\_0402\_5%

3V0

HERMTRIP#

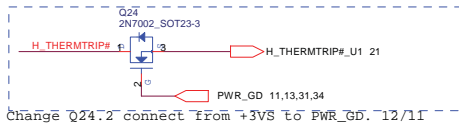
R21 1 2 0.0402\_5%

9,10,12,14,26 SMB\_DATA\_S3

Add PD R211 for FAN\_PWM. 11/30

FAN\_PWM R211 1 2 10K\_0402\_5%

[ Install R133. 7/714 ]



Layout note:  
1. Place Q1 close to bottom DDR DIMM.

Layout Note:  
place near the hottest spot area for NB & top SODIMM.

Change from +1.5V. 7/8

VCCP.1.5VSPWRGD

R33 1.5K 0402 1%

R34 1.750 0402 1%

VDDPWRGOOD\_R

Change R33, R34 value. 7/10

**Intel S3**

**CLOCKS**

JCPU1B  
COMP3  
COMP2  
COMP1  
COMP0  
SKTOCC#  
SKTOCC#

**THERMAL**

CATERR#  
PROCHOT#  
THERMTRIP#

**PWR MANAGEMENT**

RESET\_OBS#  
PM\_SYNC  
VCCPWRGOOD\_1  
VCCPWRGOOD\_0  
SM\_DRAMPWRCK  
VTTTPWRGOOD  
TAPPIWRGOOD  
RSTIN#

**JTAG & DATA**

IC\_AUB\_CFD\_rPGA\_R1P

**Power Management Signals:**

- H\_CPUREST#
- H\_PM\_SYNC
- H\_CPUPWRGD
- VCCPWRGOOD\_1
- VCCPWRGOOD\_0
- SM\_DRAMPWRCK
- VTTTPWRGOOD
- H\_PWRGD\_XDP
- PLT\_RST#

**Resistors and Connections:**

- R24, R25, R26, R27, R28, R30, R31, R32, R33, R34
- VDDPWRGOOD\_R
- VDDPWRGOOD\_0
- VDDPWRGOOD\_1

**Other Signals:**

- PRDY#
- FREQ#
- TCK
- TMS
- TRST#
- TDO
- TDI
- TDO\_M
- DBR#
- BPM#0
- BPM#1
- BPM#2
- BPM#3
- BPM#4
- BPM#5
- BPM#6
- BPM#7

VDDPWGOOD\_R R751 2  1 @ 1.1K\_0402\_1% +1.5VS\_CPU\_VDDQ

Figure 1: Pin connection diagram of the JCFAN1 module. The diagram shows a 4-pin module with pins 1, 2, 3, and 4. Pin 1 is connected to a +3V5 supply through a 10K 0.02.5% resistor (R40). Pin 2 is connected to a +5V5 supply through a 10K 0.02.5% resistor (R41). Pin 3 is connected to a +5V5 supply. Pin 4 is connected to a +5V5 supply. The module is labeled 'JCFAN1' and 'CONN@ ACES\_50273-0040N-001'. A note states 'No install R41.'

Pin connection diagram for SAMTE\_BSH-030-01-L-D-A connector. The diagram shows a 60-pin connector with pins numbered 1 to 60. Pins 1-17 are labeled GND0, OBSFN\_A0, OBSFN\_F1, GND2, OBSDATA\_A0, OBSDATA\_A1, GND4, OBSDATA\_A2, OBSDATA\_A3, OBSFN\_B0, OBSFN\_B1, GND6, OBSDATA\_B0, OBSDATA\_B1, GND10, OBSDATA\_B2, OBSDATA\_B3, GND12, PWRGOOD/HOOK0, HOOK1, VCC\_OBS\_AB, HOOK2, HOOK3, GND14, SDA, SCL, TCK1, TCK0, GND16, and GND17. Pins 18-37 are labeled GND0, OBSFN\_C0, OBSFN\_F1, GND2, OBSDATA\_C0, OBSDATA\_C1, GND4, OBSDATA\_C2, OBSDATA\_C3, OBSFN\_D0, OBSFN\_D1, GND6, OBSDATA\_D0, OBSDATA\_D1, GND10, OBSDATA\_D2, OBSDATA\_D3, GND12, ITPCLK/HOOK5, ITPCLK/HOOK6, VCC\_OBS\_CD, RESET/HOOK6, DBR/HOOK7, GND15, TD0, TRST#, TDI, TMS, and GND17. Pins 38-57 are labeled CLK\_CPU\_XDP, CLK\_CPU\_XDP#, XDP\_RST#\_R, XDP\_DBRESE#\_R, XDP\_TDO, XDP\_TRST#, XDP\_TDI, and XDP\_TMS. Pins 58-60 are labeled CF68, CF69, CF60, CF61, CF62, CF63, CF610, CF611, CF64, CF65, CF66, and CF67. The diagram also shows a VCCP pin connected to pin 58. A note indicates a swap of 02/25 for pins 58 and 59. A legend at the bottom shows RST#\_R, PLT\_RST#, and PLT\_RST# connections.

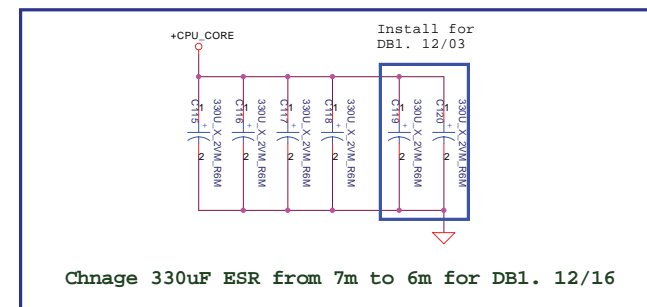
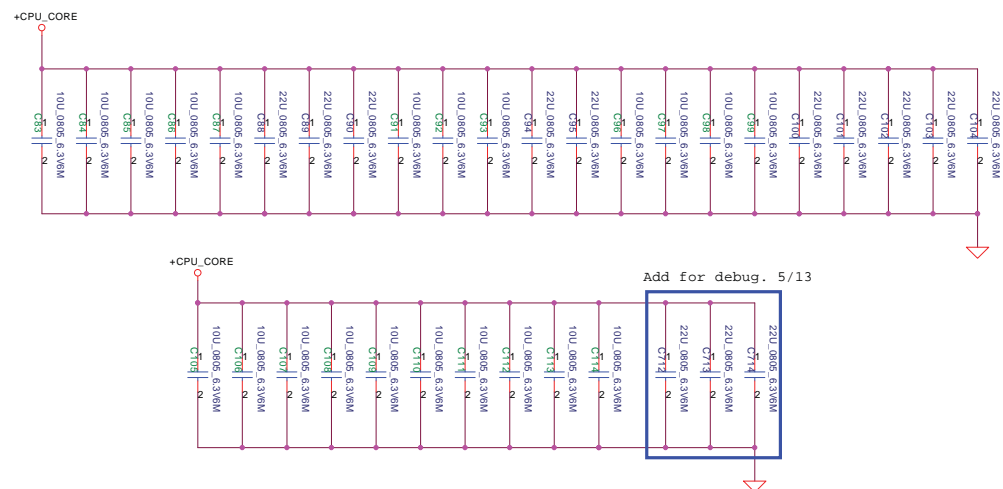
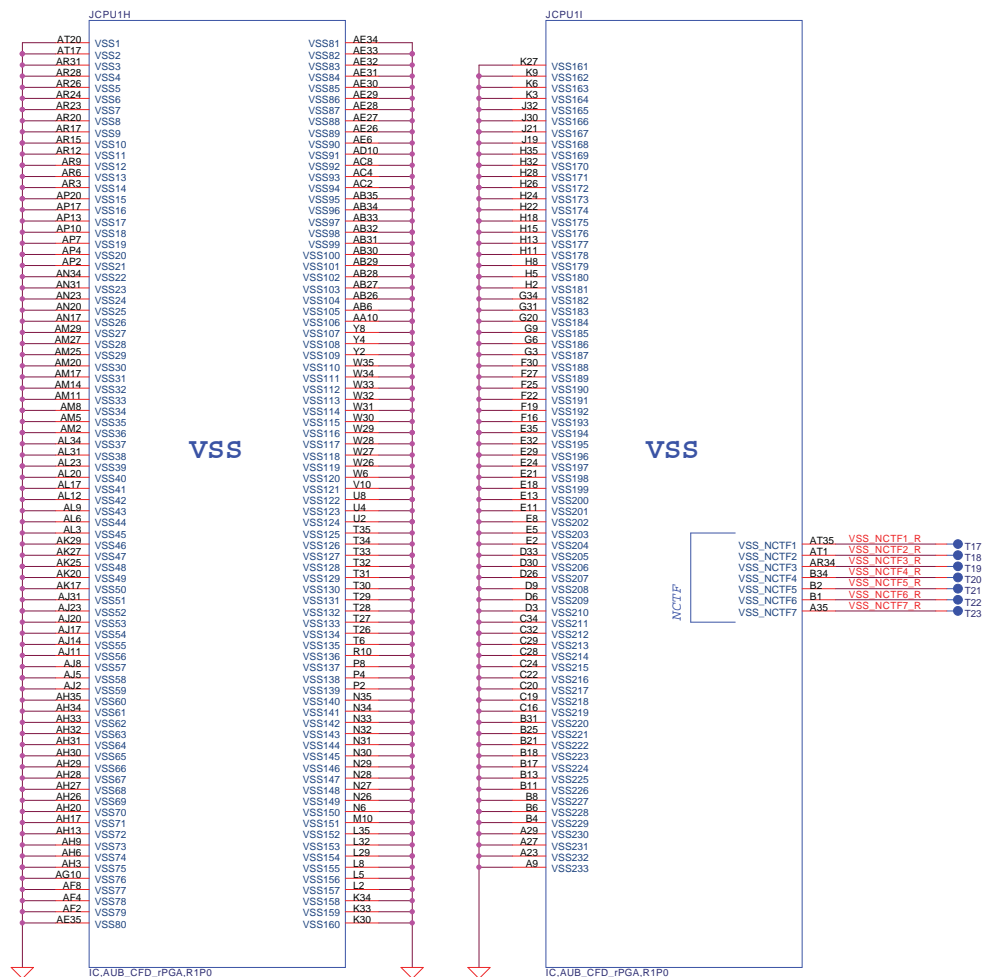
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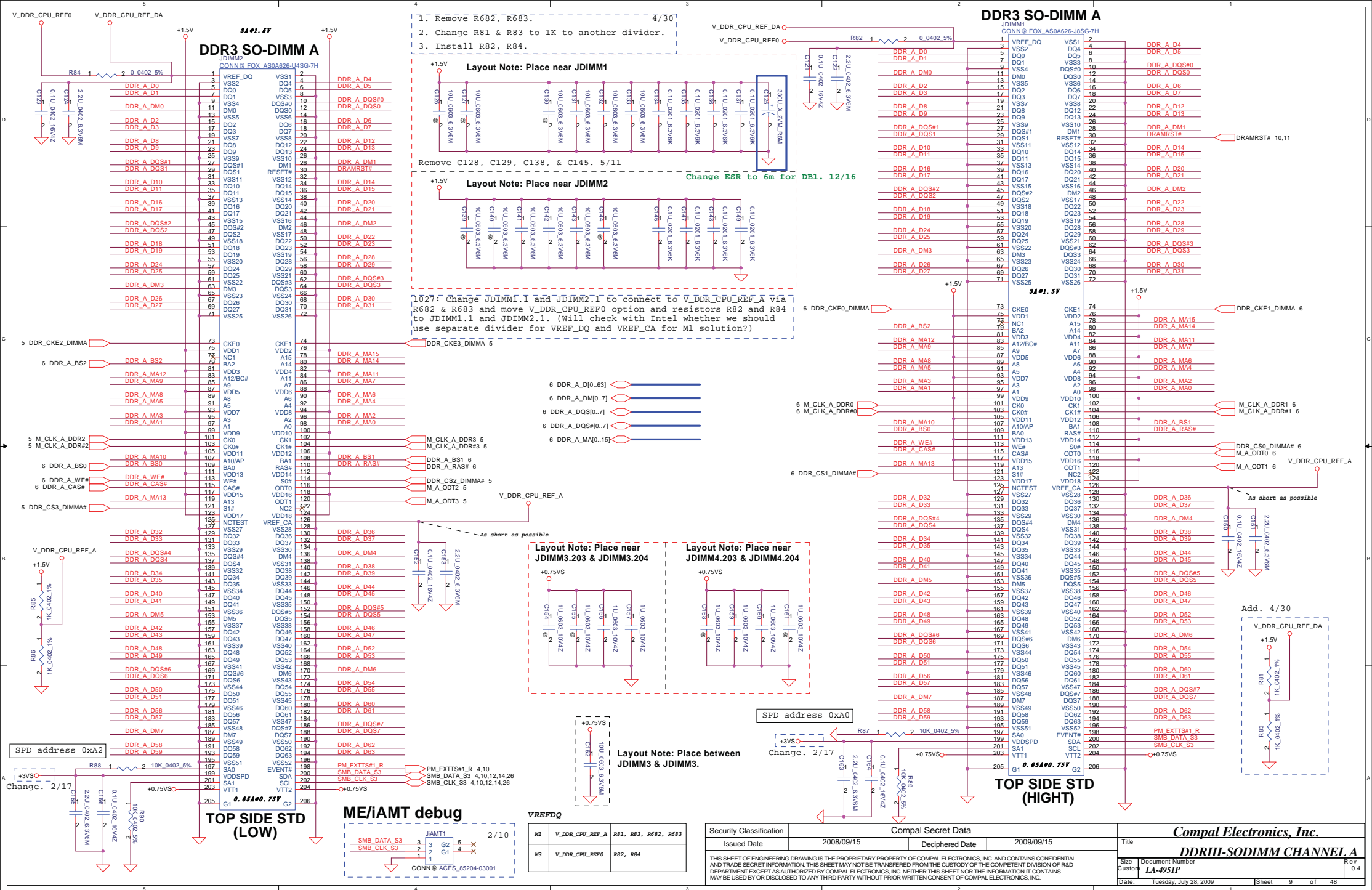




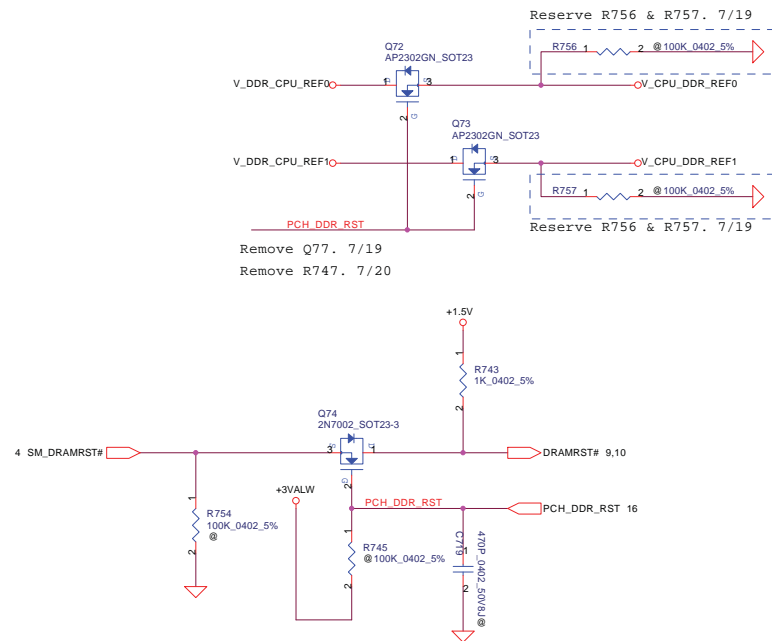


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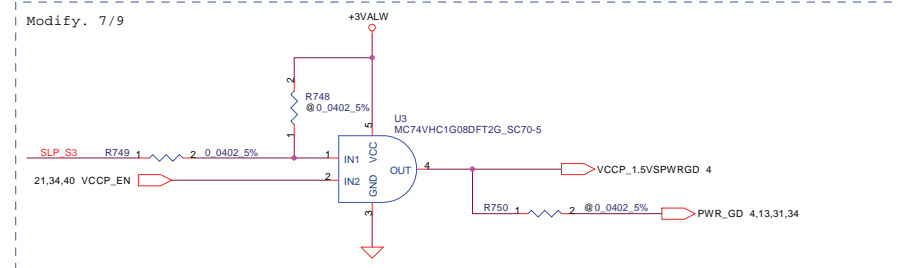
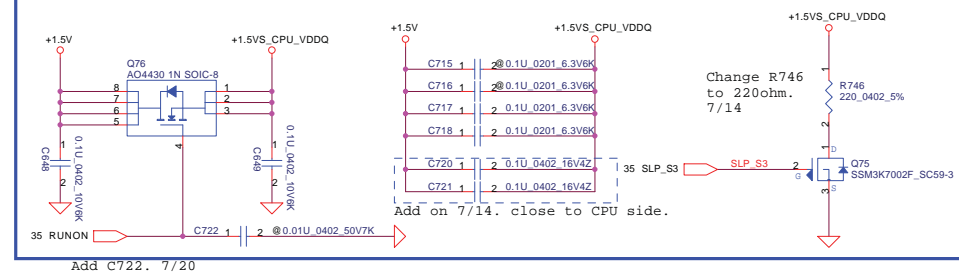








## +1.5V to +1.5VS\_CPU\_VDDQ Transfer

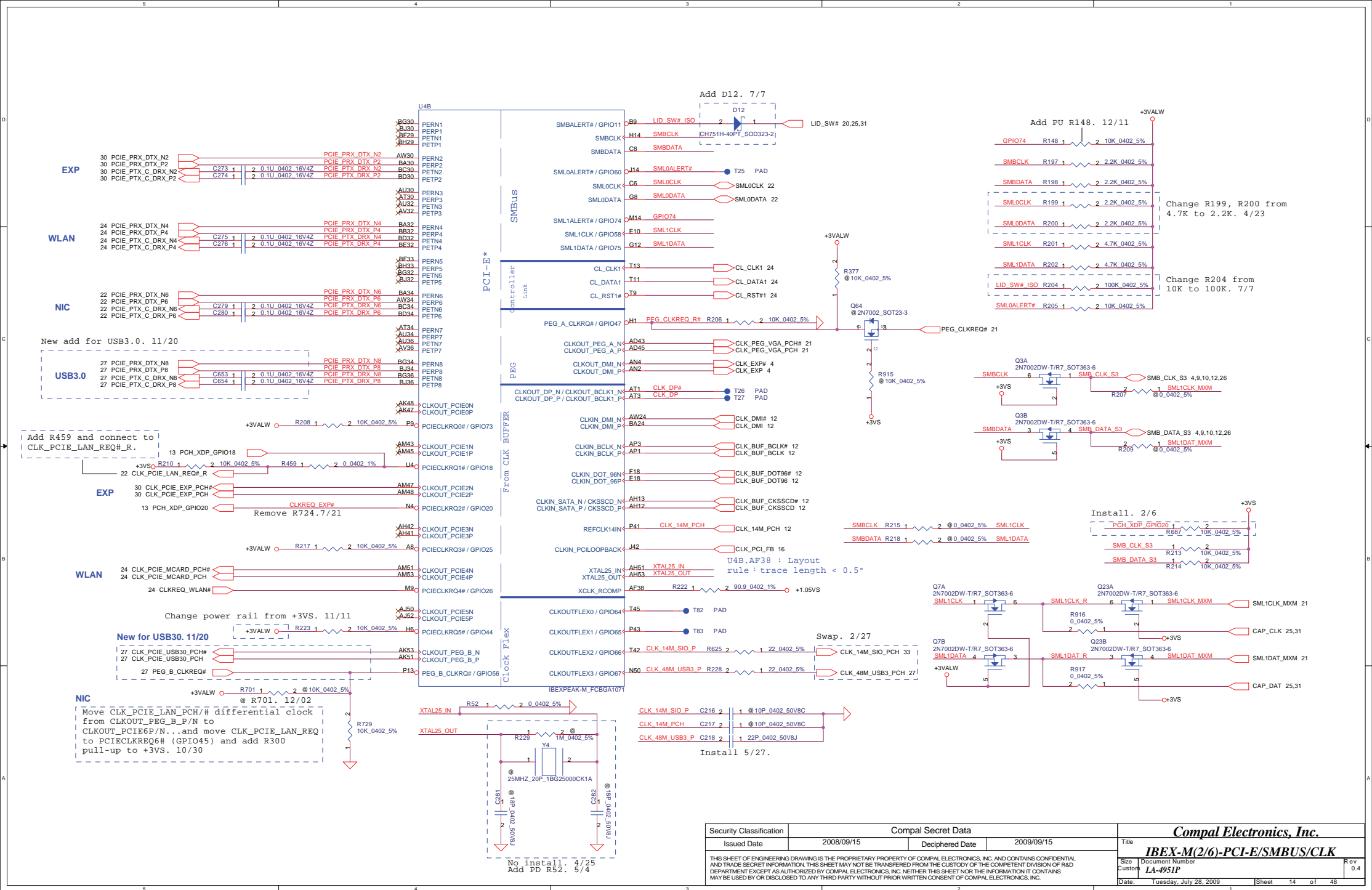


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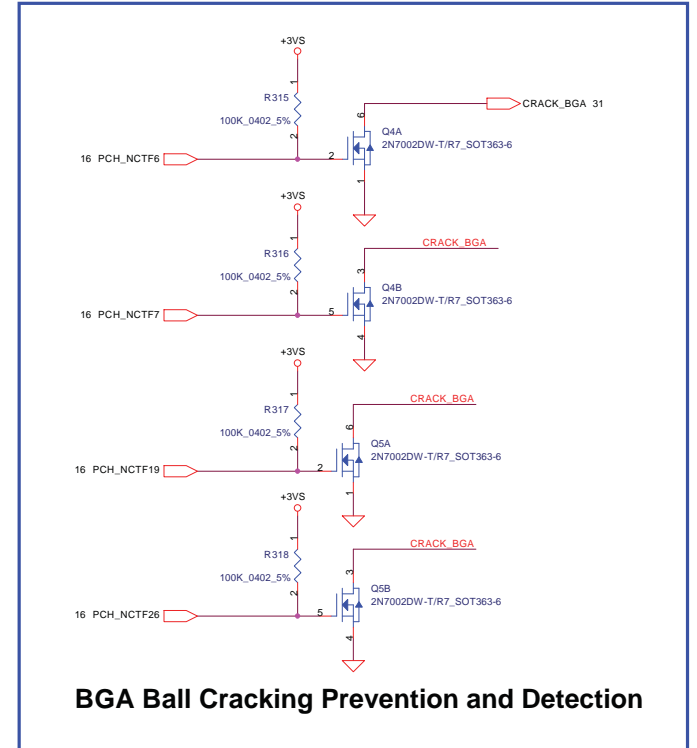
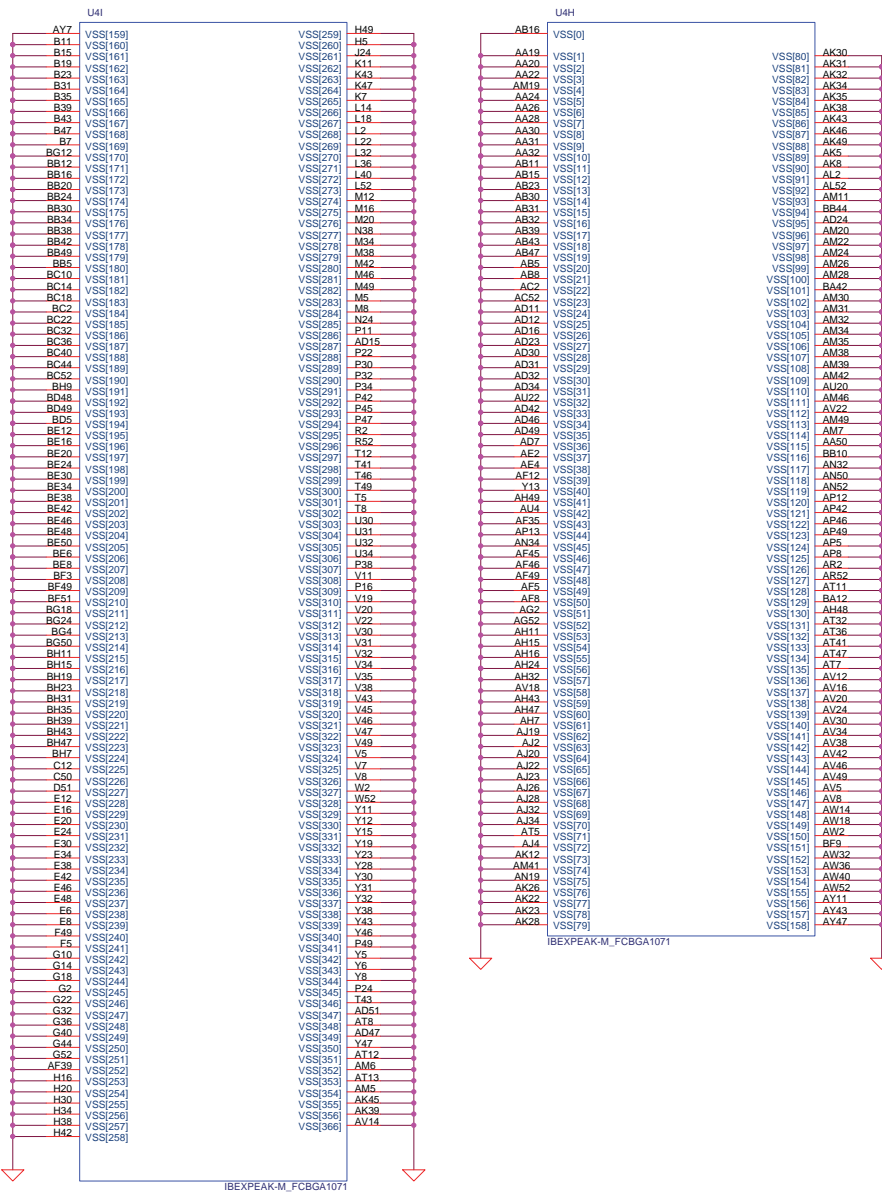






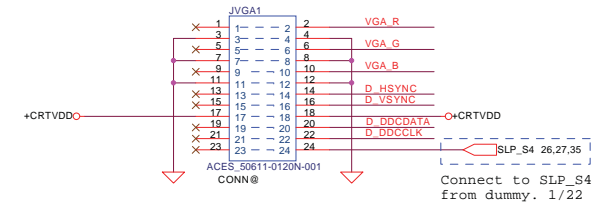
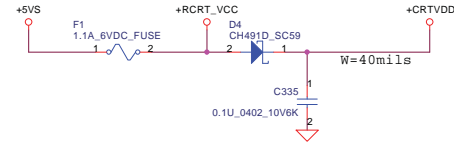
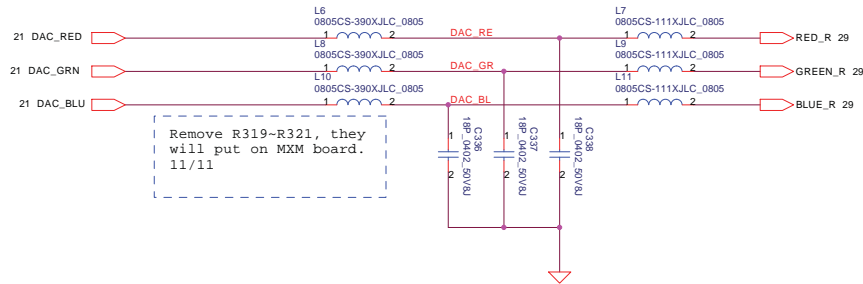




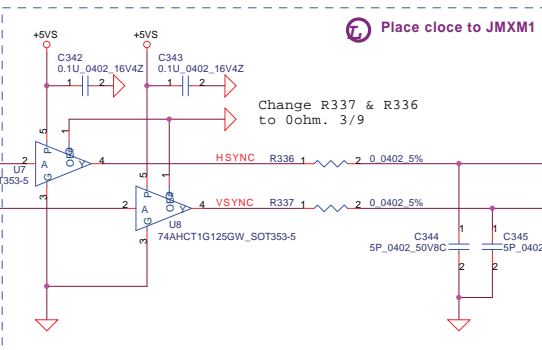
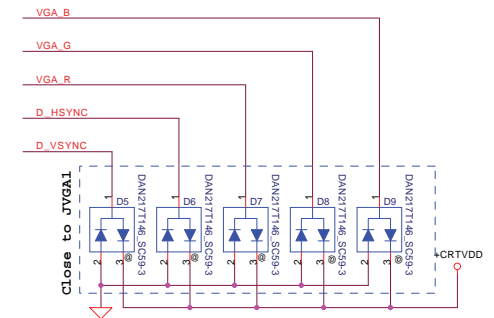
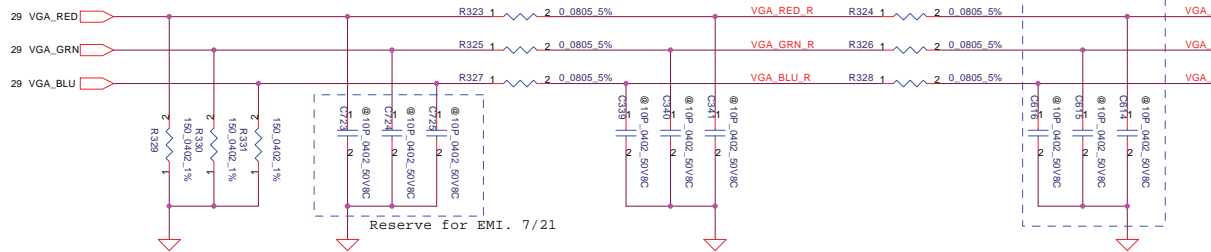


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Place close to JMXM1

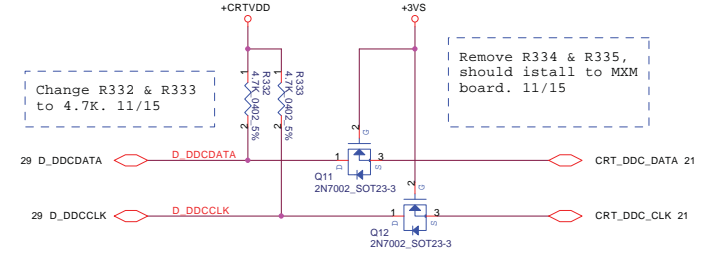


Add C614~C616 for Nvidia request. 11/15



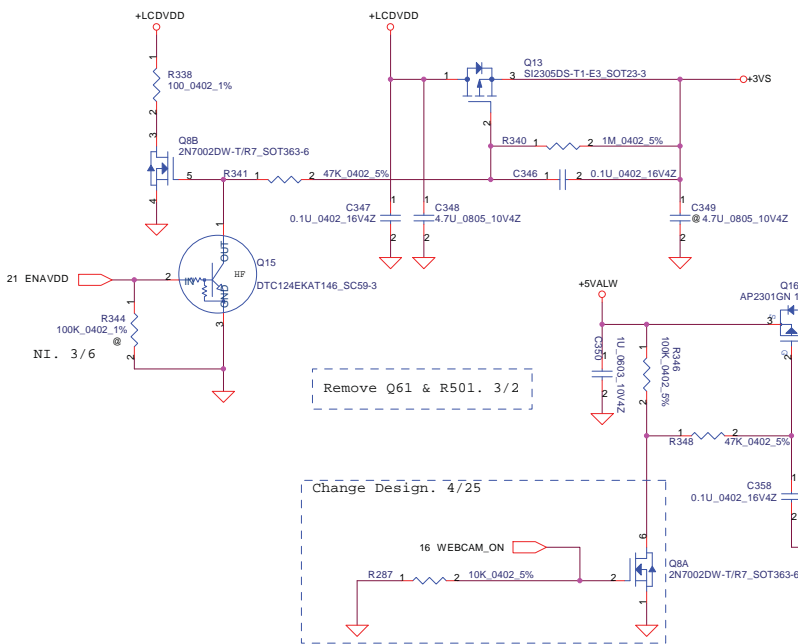
D\_HSYNC & D\_VSYNC should be routed to docking connector then to VGA connector

Change R332 & R333 to 4.7K. 11/15



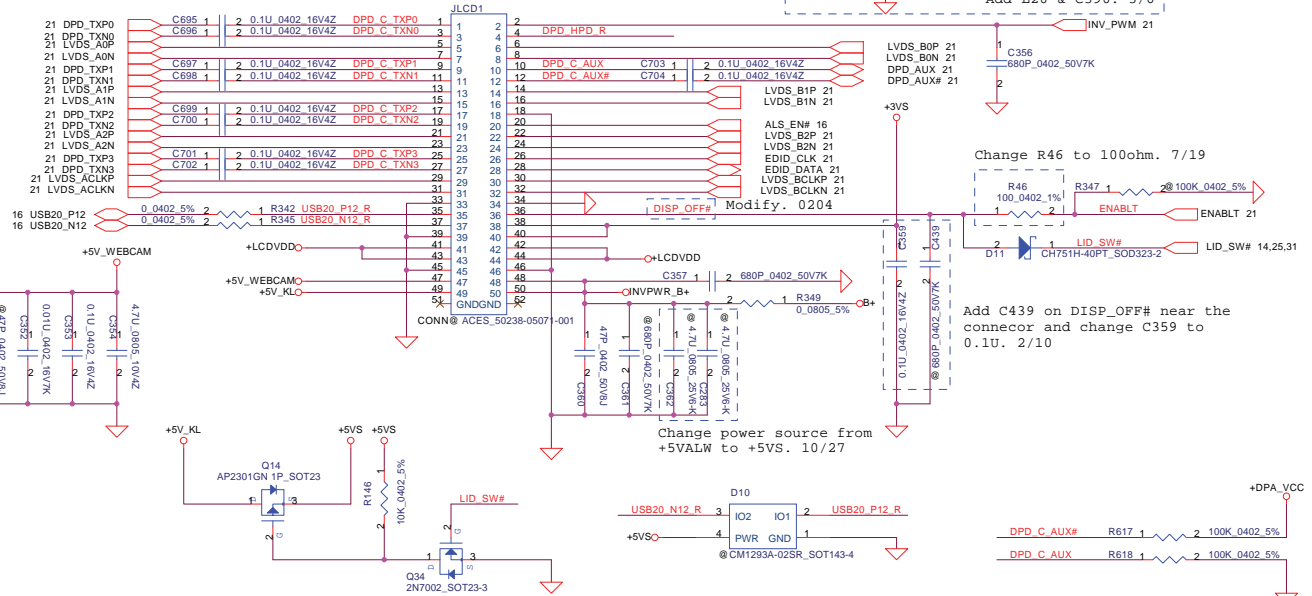
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## LCD POWER CIRCUIT

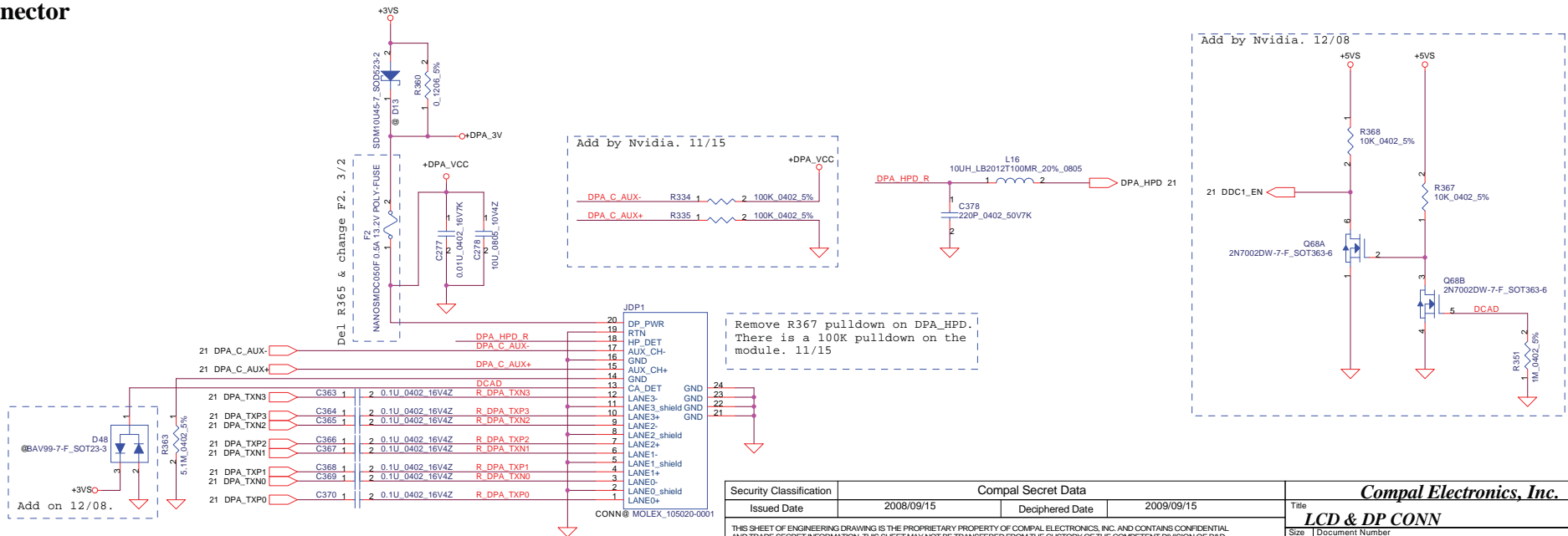


## LCD/PANEL BD. CONN.

Modify pin assignment. 2/23



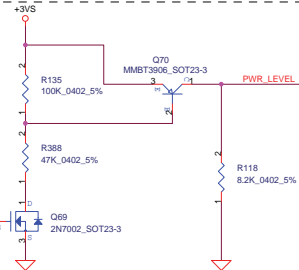
## Display port Connector



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Remove Q19 & R376. 2/24  
Remove C377. 7/10

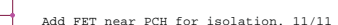


31,35,38,44 ADP\_PRES  2 Q69  
G 2N7002\_SOT23-



## 29 Docking

Change to dummy. 12/22

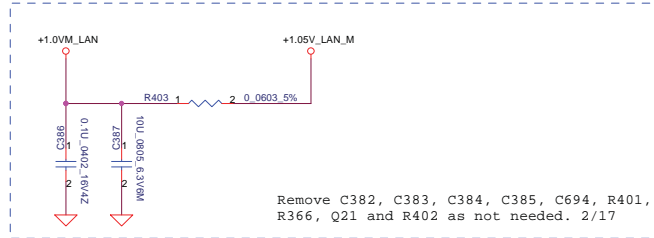
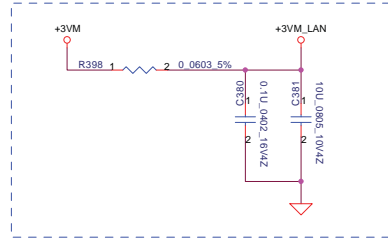


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Change R394 to NI and install R381

<http://hobi-elektronika.net>

Update on 10/27.



Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402 as not needed. 2/17

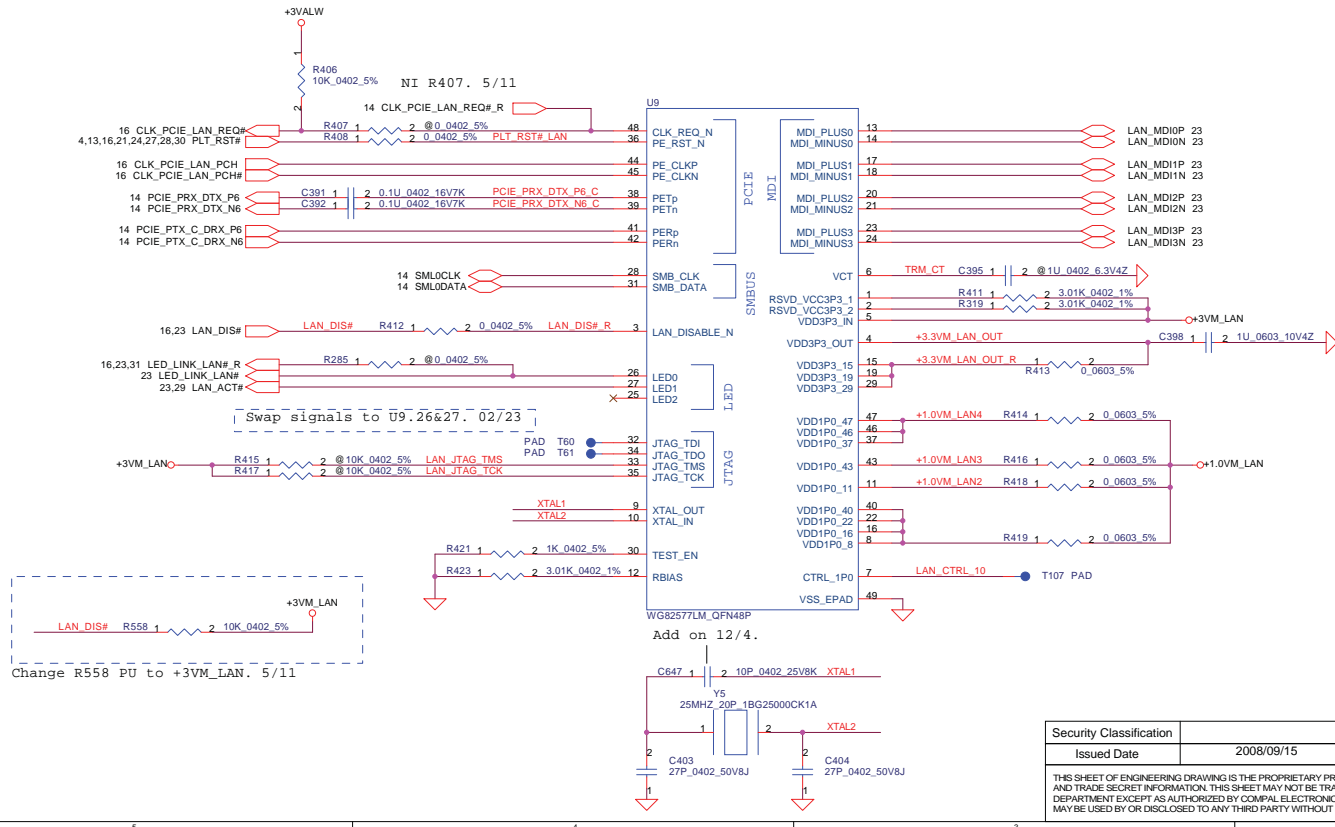
Remove note. 0205

Remove C388, C389, C390, & C393 on +1.0VM\_LAN; Remove C394, C396 & C397 on +3.3VM\_LAN\_OUT\_R; Remove C399 & C400 on +1.0VM\_LAN4; Remove C401 on +1.0VM\_LAN3; and Remove C402 on +1.0VM\_LAN2 as done in Intel's RedFort CRB

Remove Q17, R124, and R405 (Intel confirmed isolation not required for Hanksville)

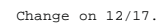
2/23

Remove R354, R355, Q22A, Q22B; and connect SML0CLK and SML0DATA directly to LAN\_SM\_CLK and LAN\_SM\_DAT. 2/23



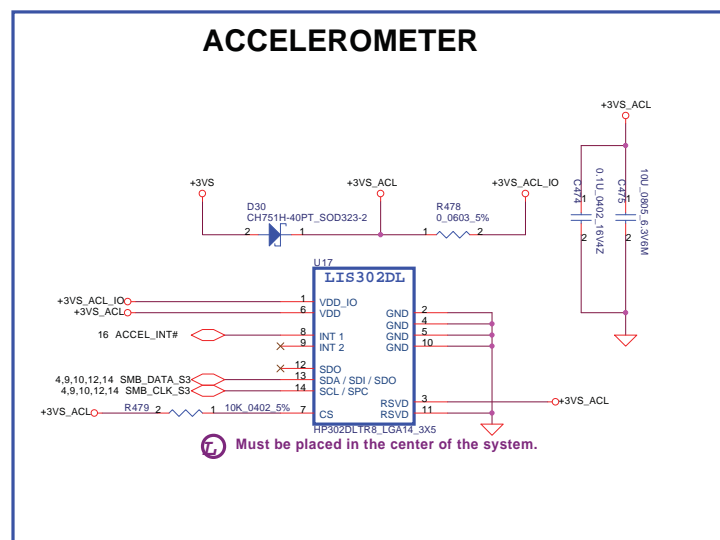
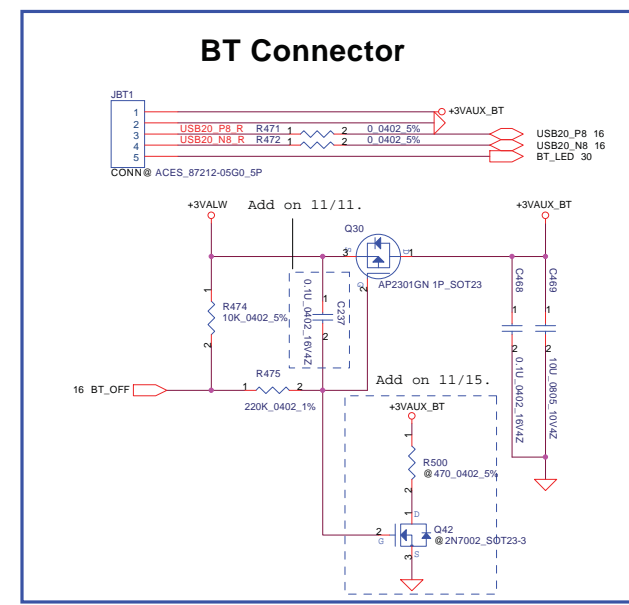
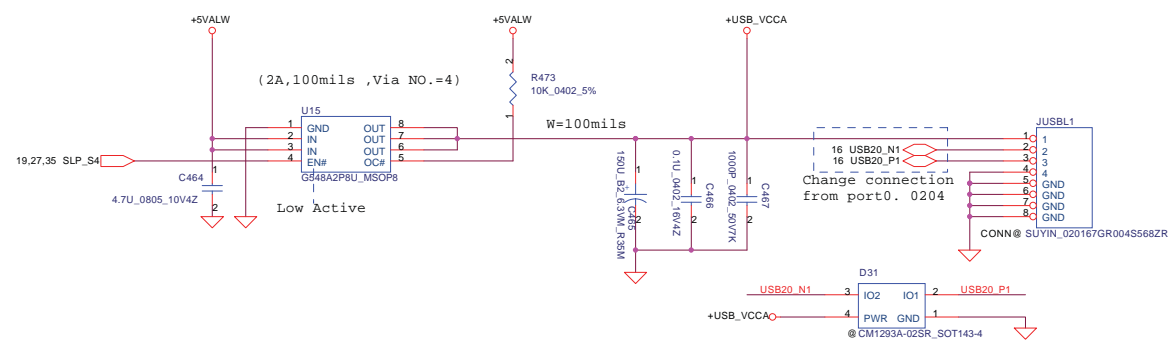
Change R558 PU to +3VM\_LAN. 5/11

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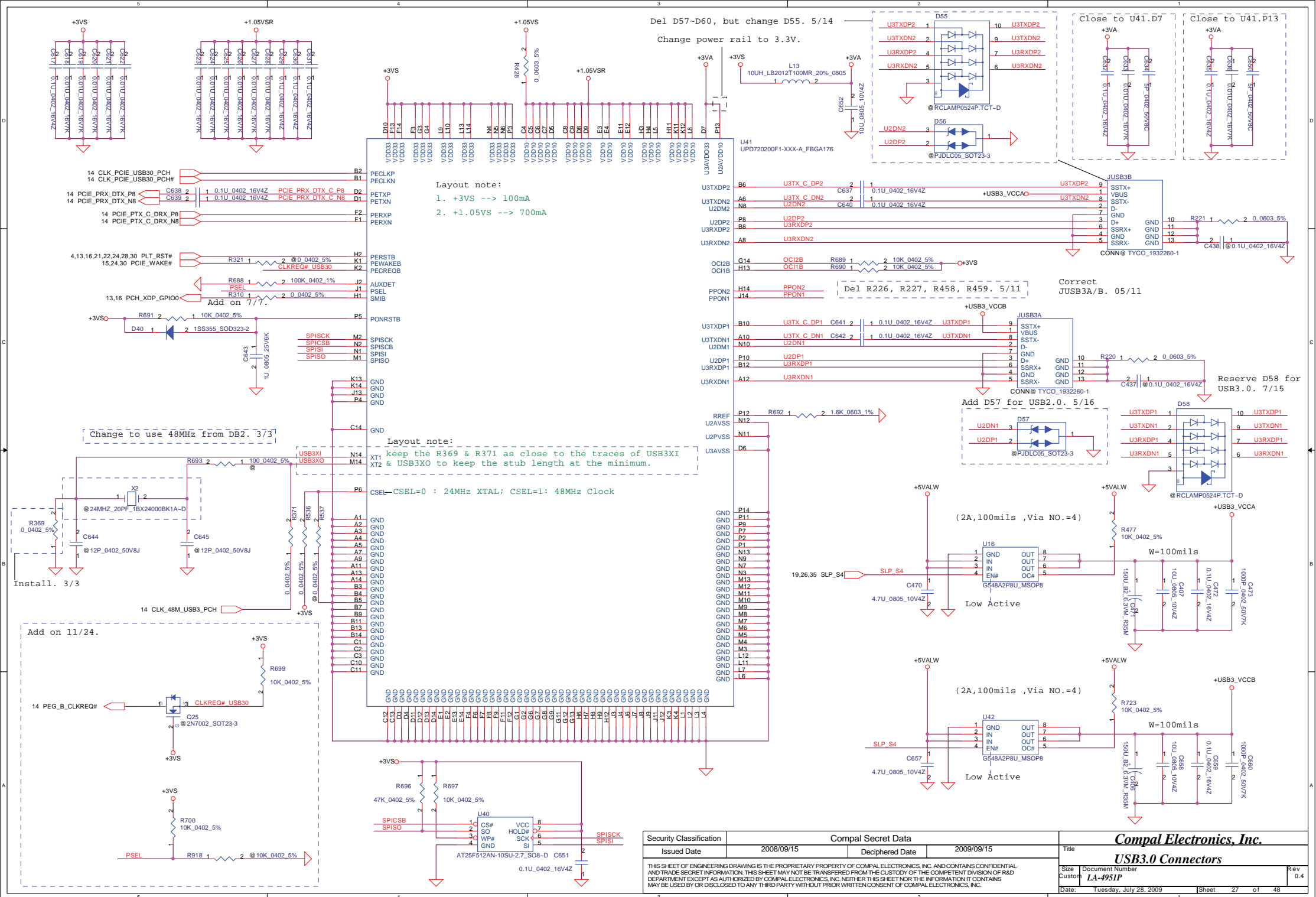






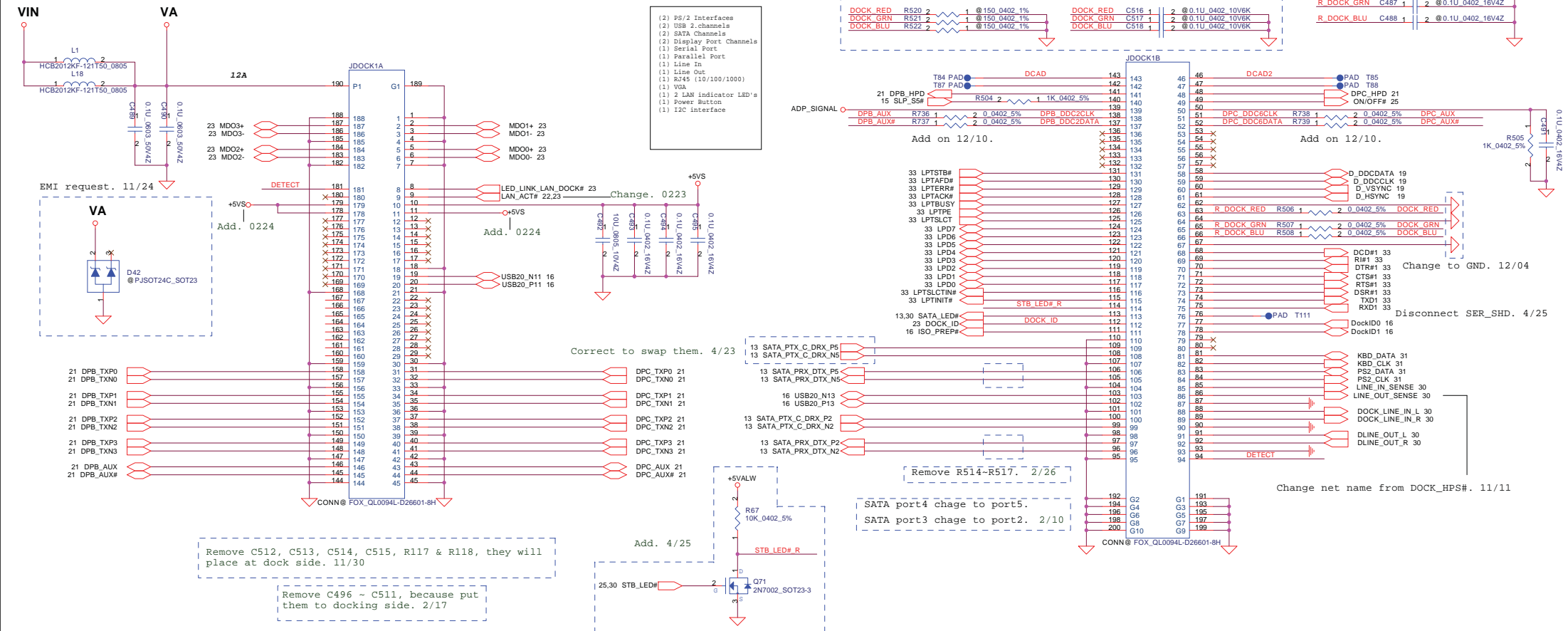
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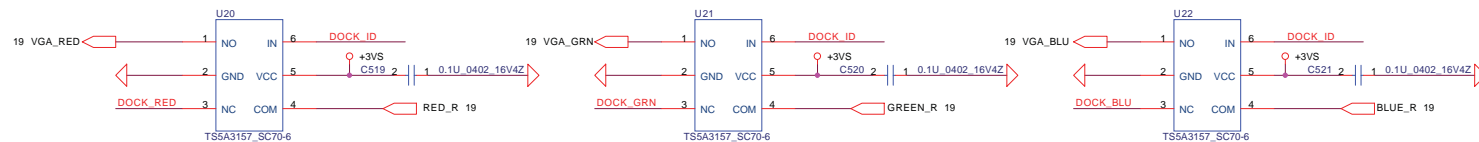


# DOCKING CONNECTOR (190 pins)

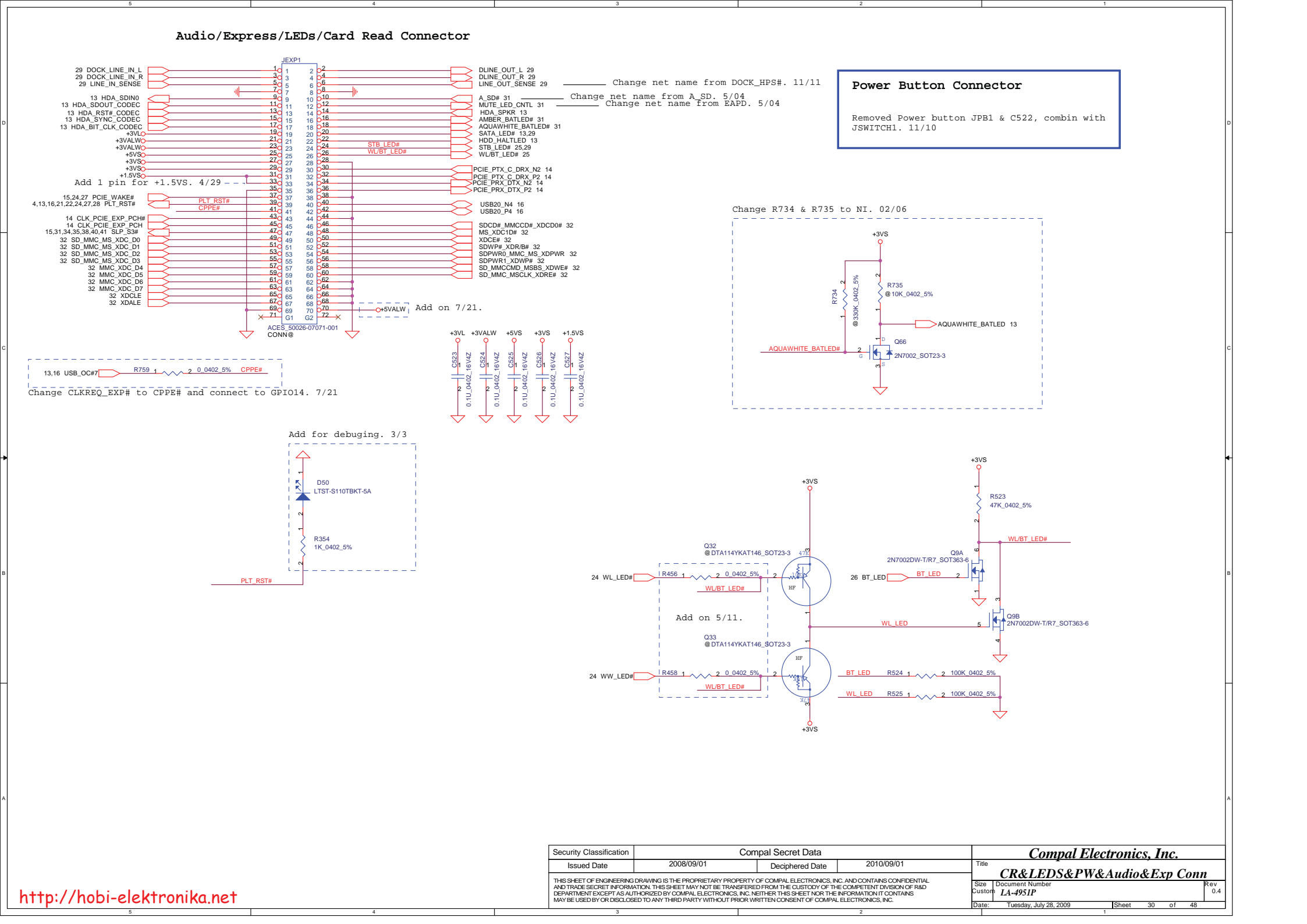
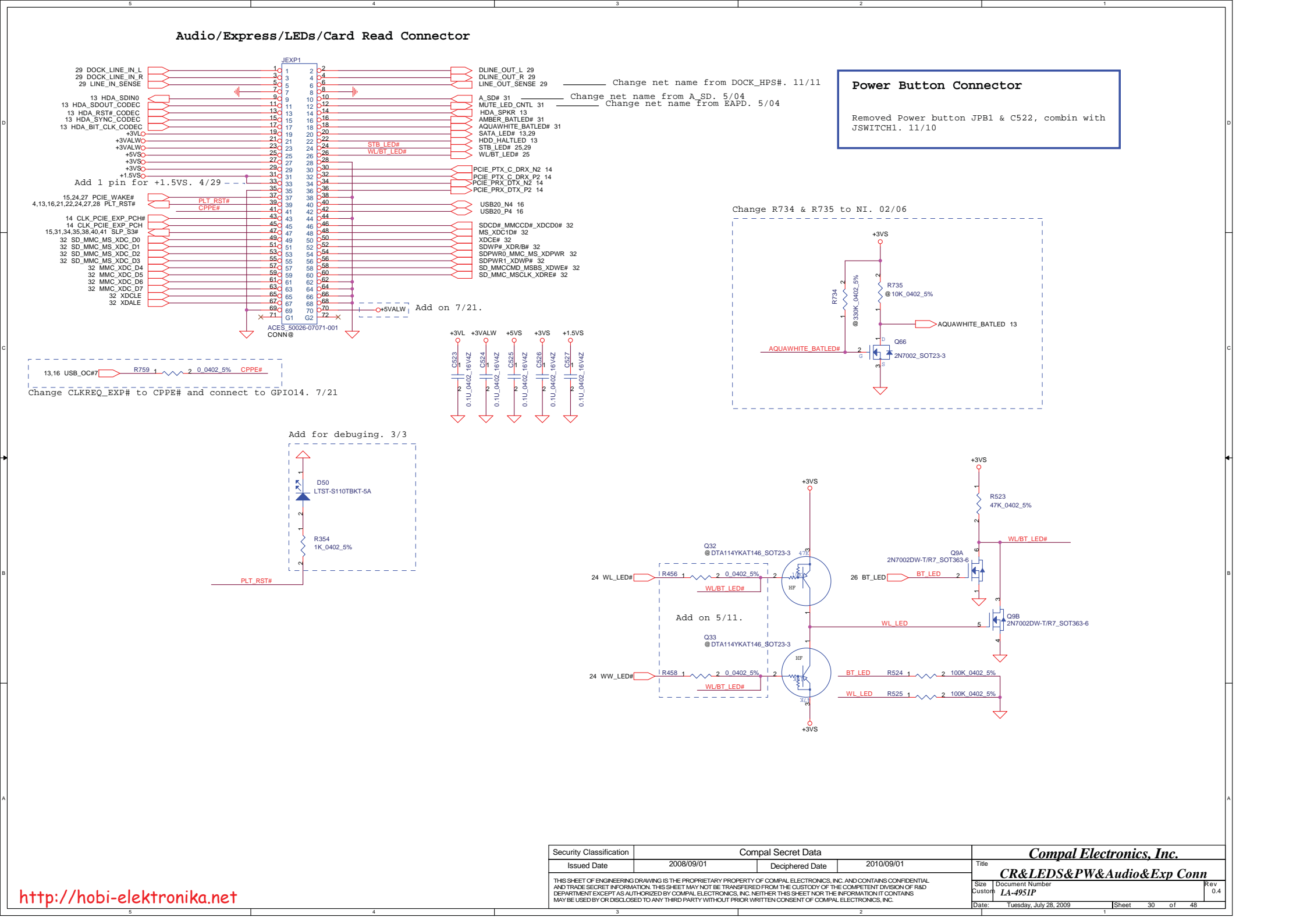
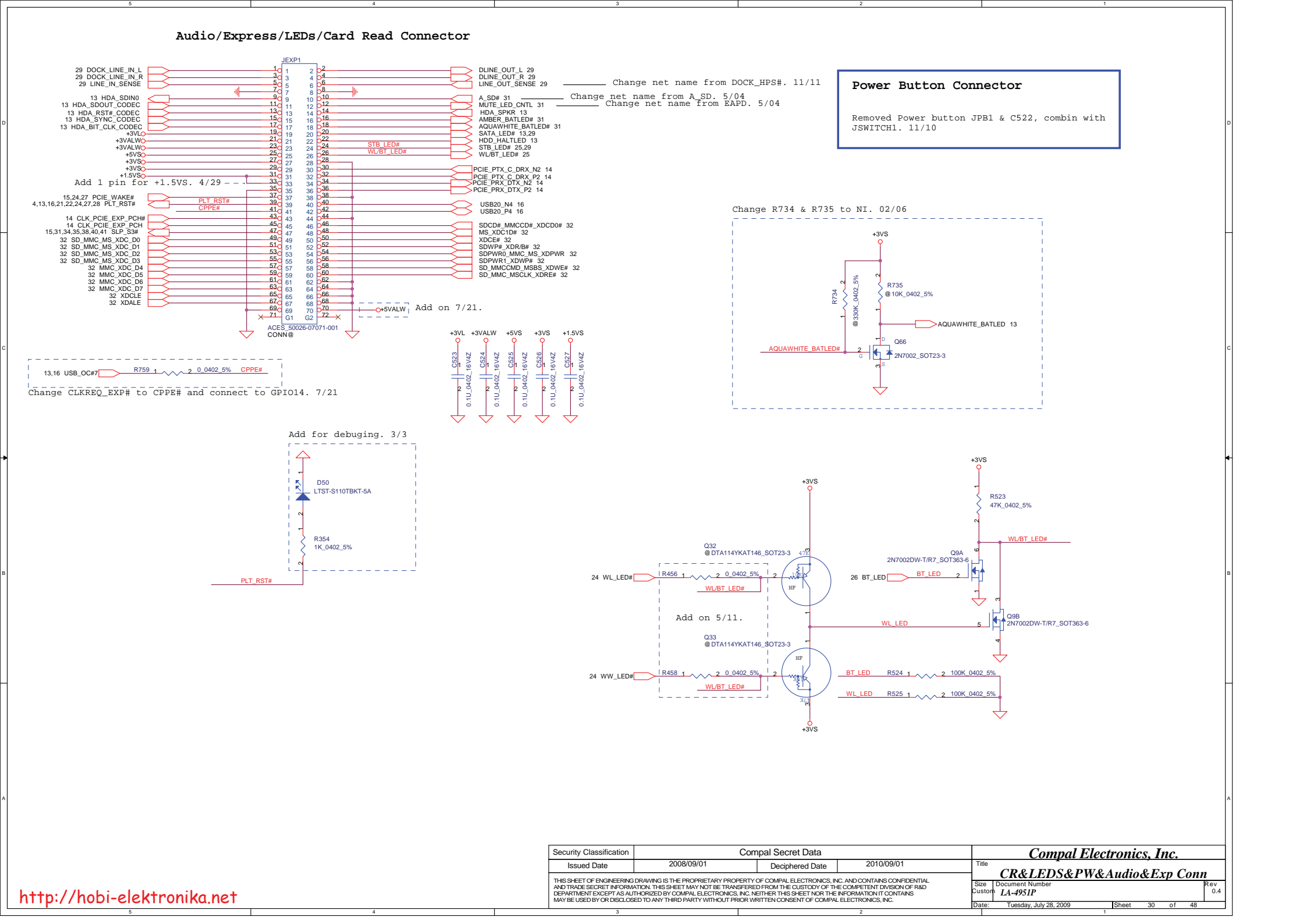
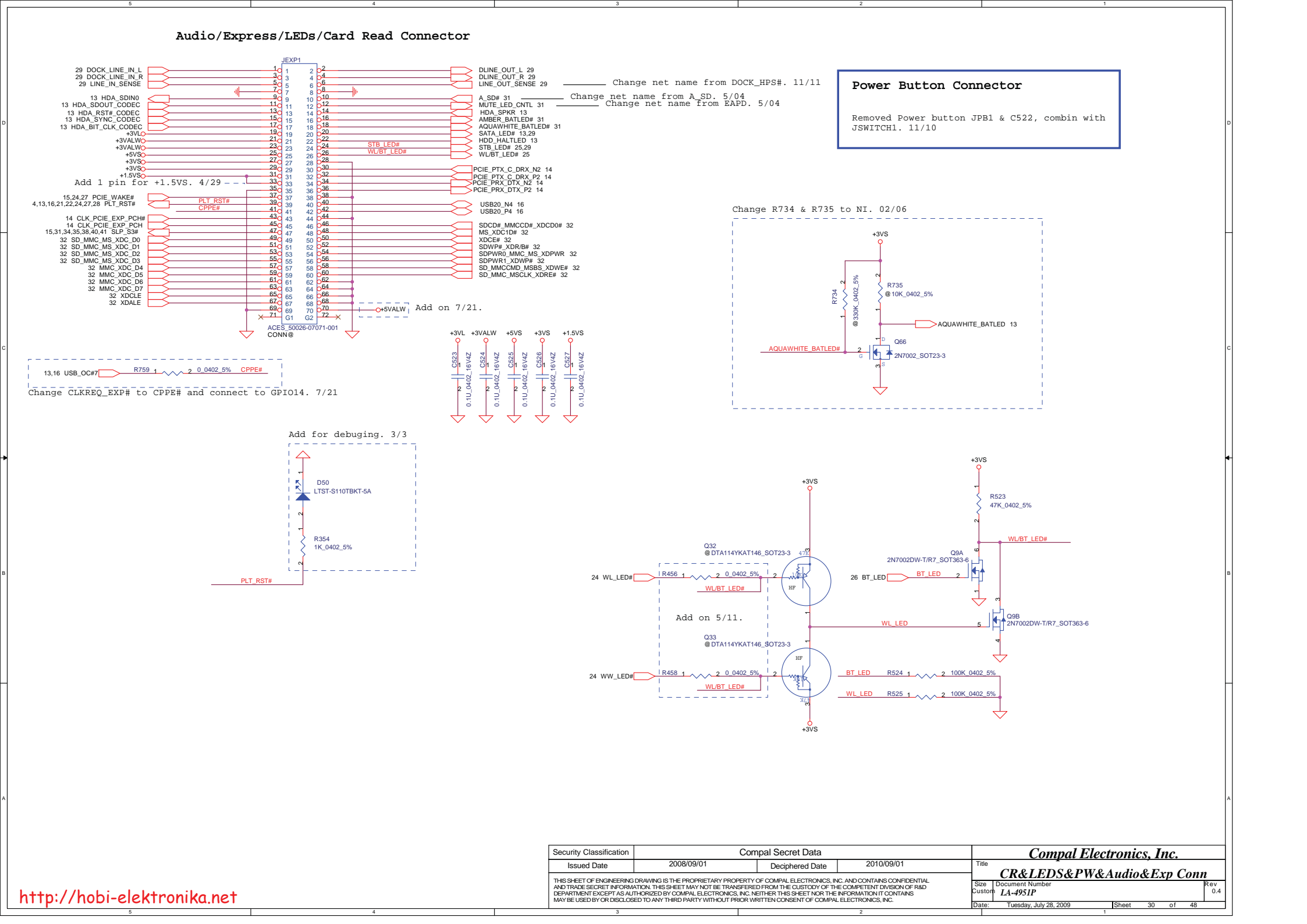


## RGB Q-Switch

IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON



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Date: Tuesday, July 28, 2009				Sheet 29 of 48

[illegible]

**Audio/Express/LEDs/Card Read Connector**

**Power Button Connector**

Removed Power button JPB1 & C522, combin with JSWITCH1. 11/10

Change R734 & R735 to NI. 02/06

Add 1 pin for +1.5VS. 4/29

Change CLKREQ\_EXP# to CPPE# and connect to GPIO14. 7/21

Add for debugging. 3/3

Add on 7/21.

Add on 5/11.

Change net name from DOKK\_HPS#. 11/11

Change net name from A\_SD. 5/04

Change net name from EAPD. 5/04

Remove Power button JPB1 & C522, combin with JSWITCH1. 11/10

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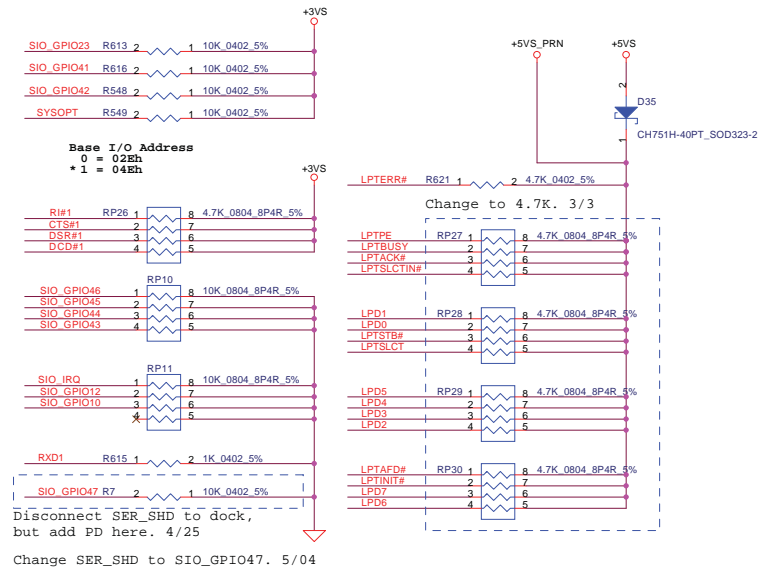
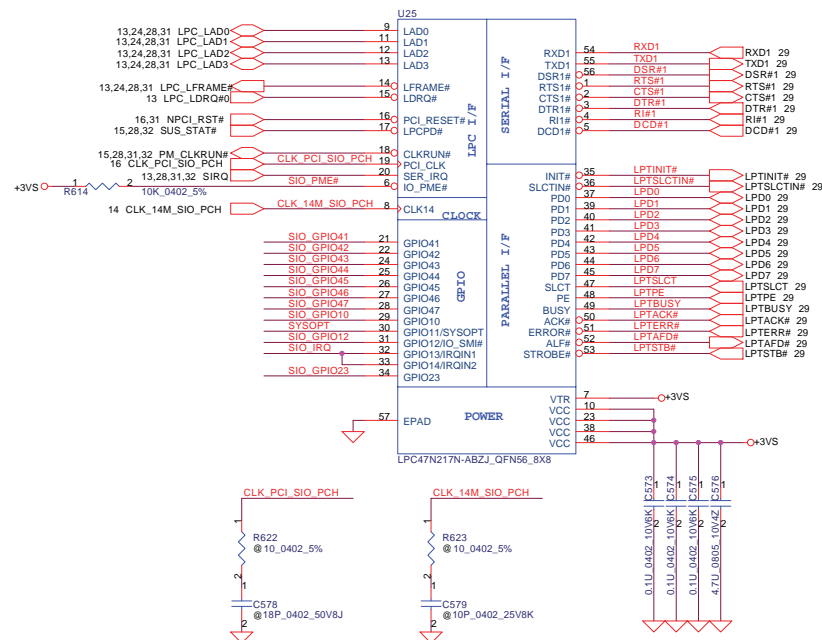
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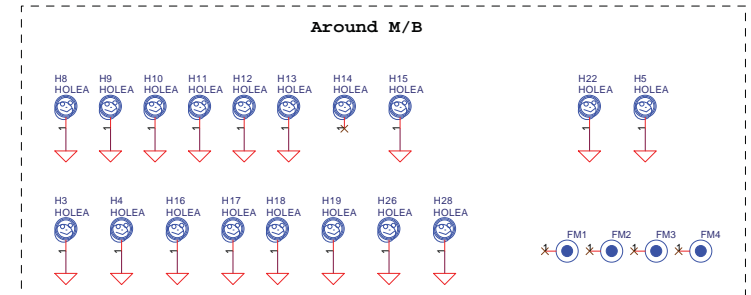
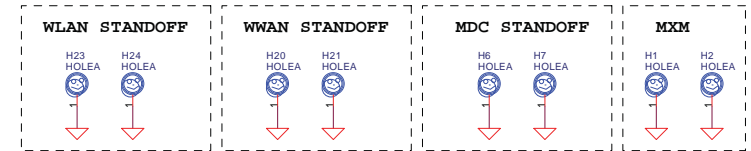
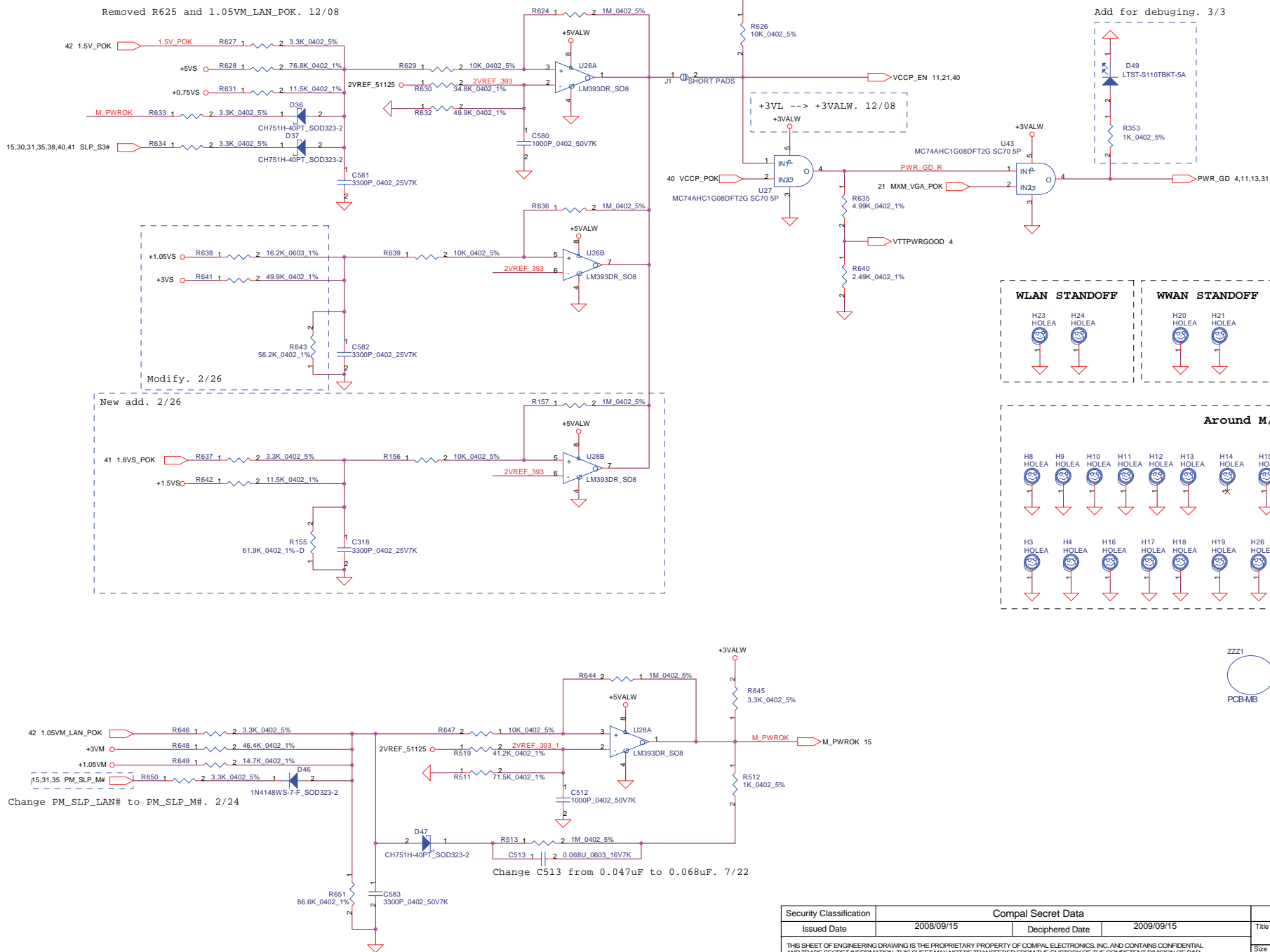








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Custom	LA-4951P	Date:	Tuesday, July 28, 2009	Sheet 33 of 48

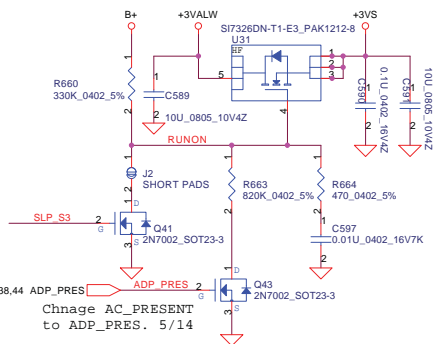


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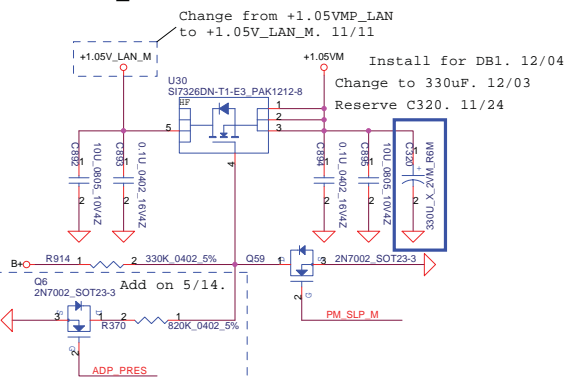
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				Sheet 34	of 48

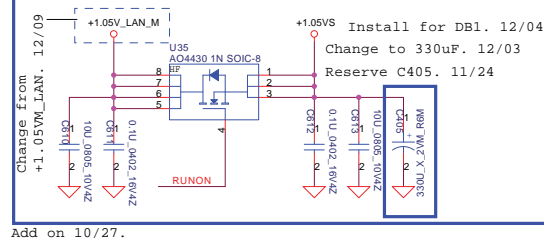
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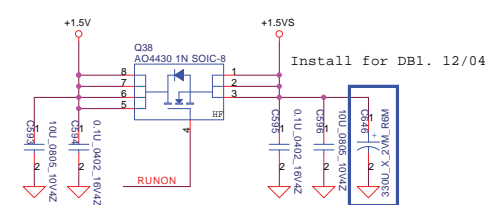
## +1.05VM\_LAN to +1.05VM Transfer



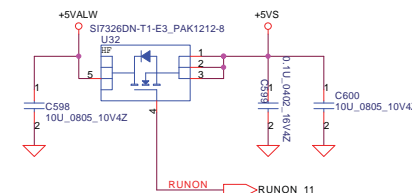
## +1.05VM to +1.05VS Transfer



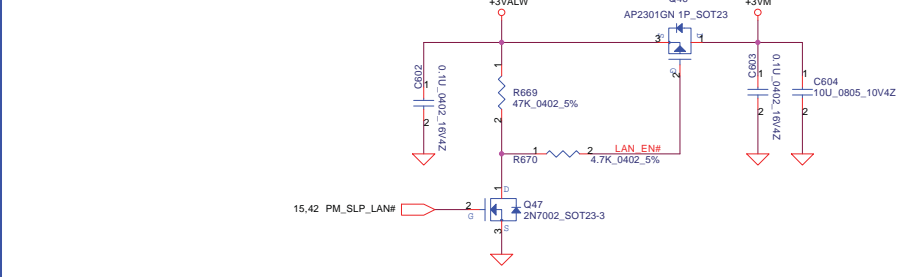
## +1.5V to +1.5VS Transfer



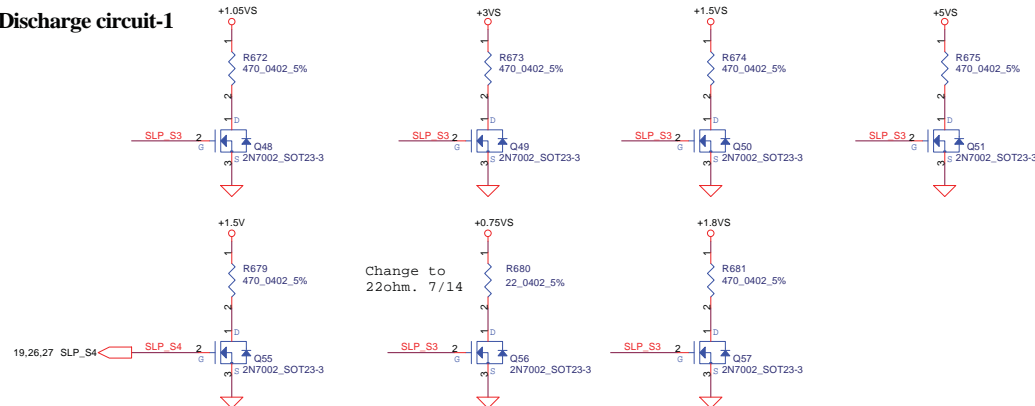
## +5VALW to +5VS Transfer



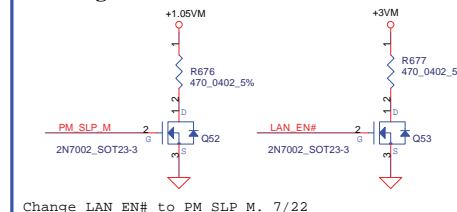
## +3VALW to +3VM Transfer



## Discharge circuit-1

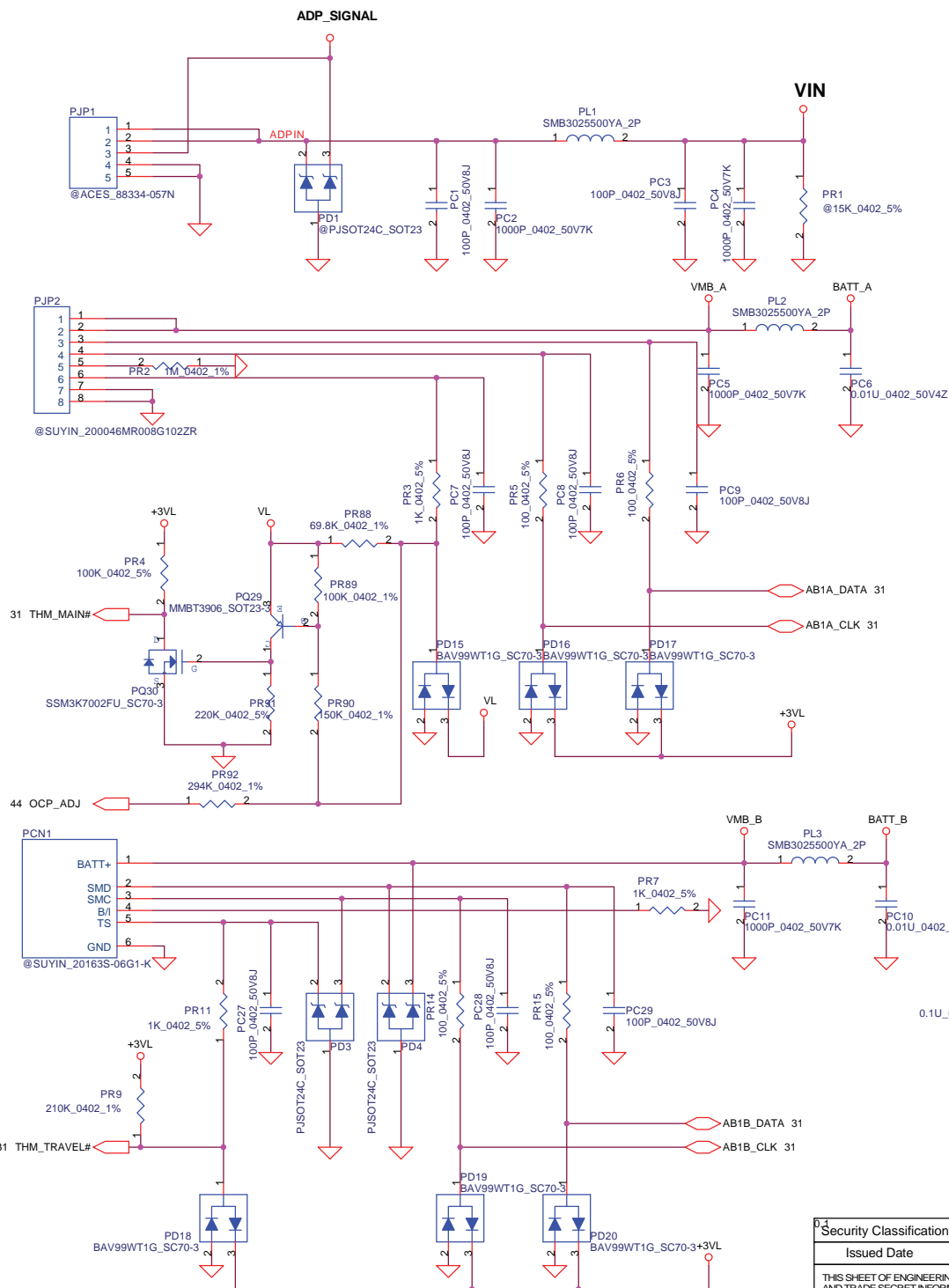


## Discharge circuit-2 for V-M

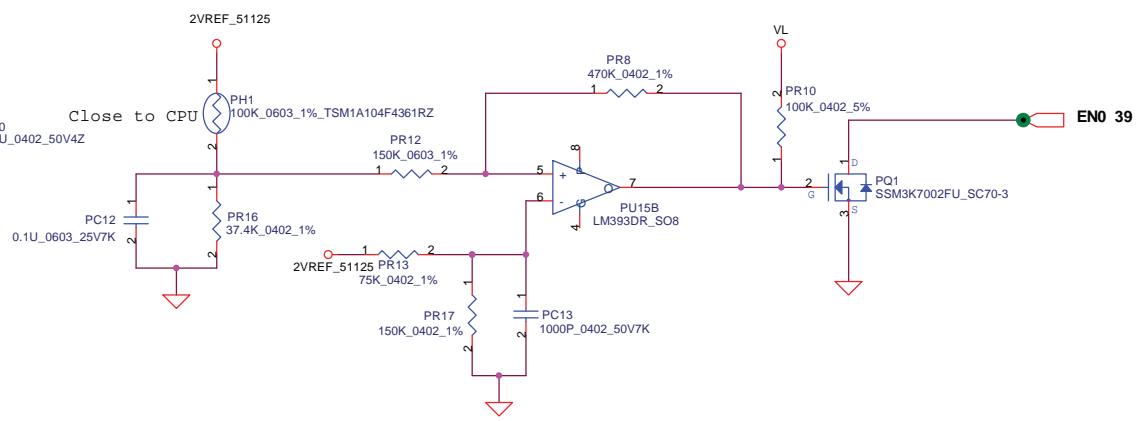


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

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				Sheet	35 of 48

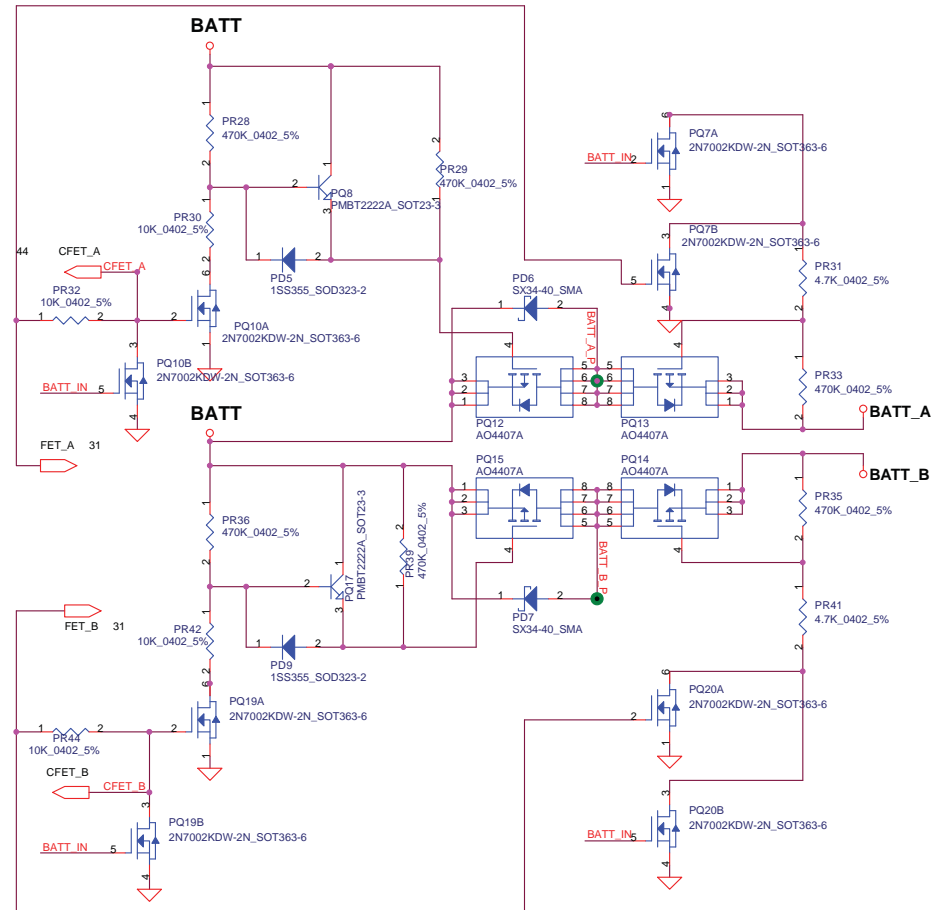
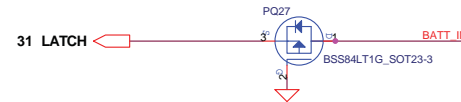
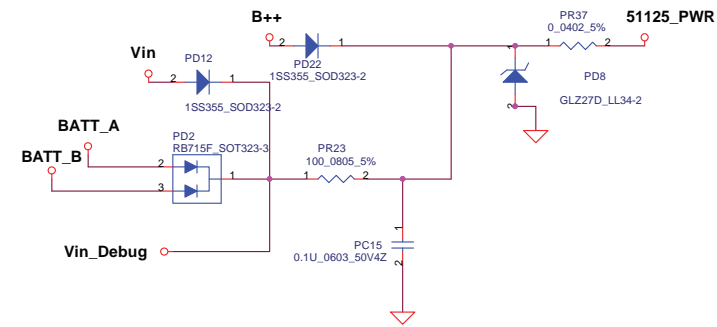
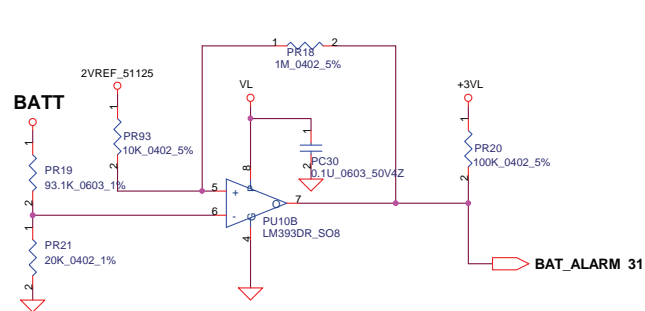


PH1 under CPU botten side :  
CPU thermal protection at 90 +-3 degree C  
(Need to be checked)



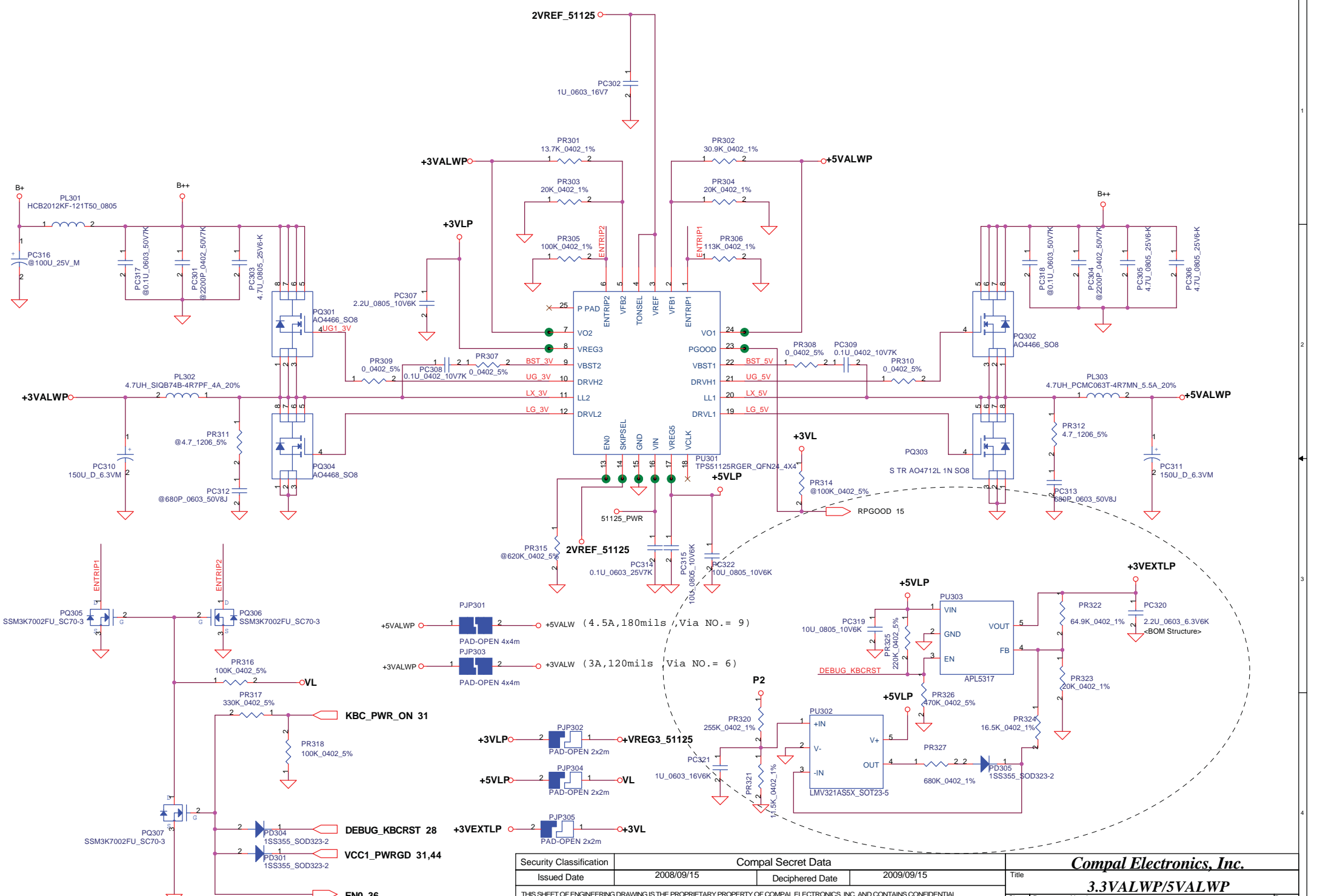
<http://hobi-elektronika.net>

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Size	Document Number	Rev		Date: Tuesday, July 28, 2009	
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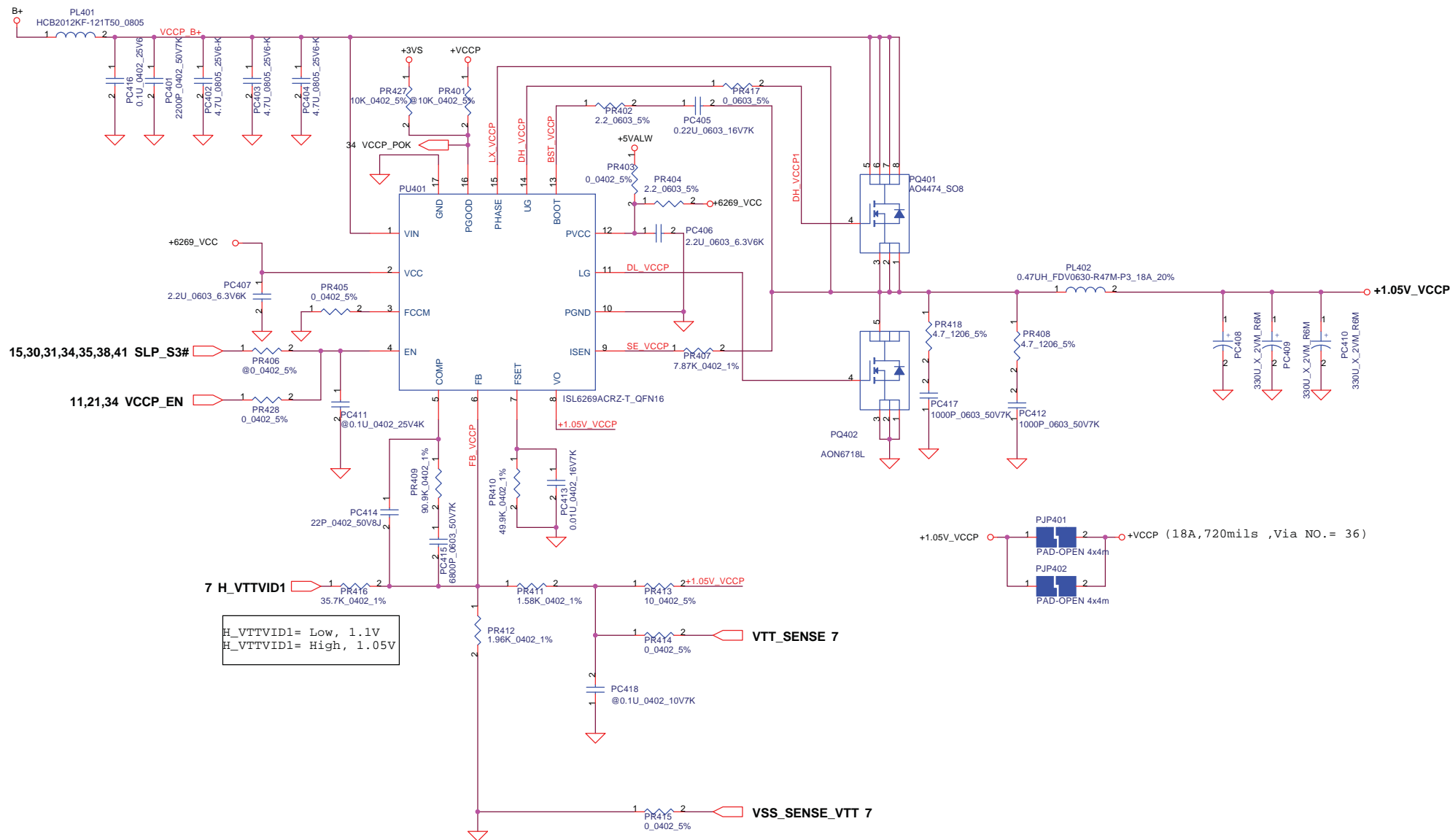




<http://hobi-elektronika.net>

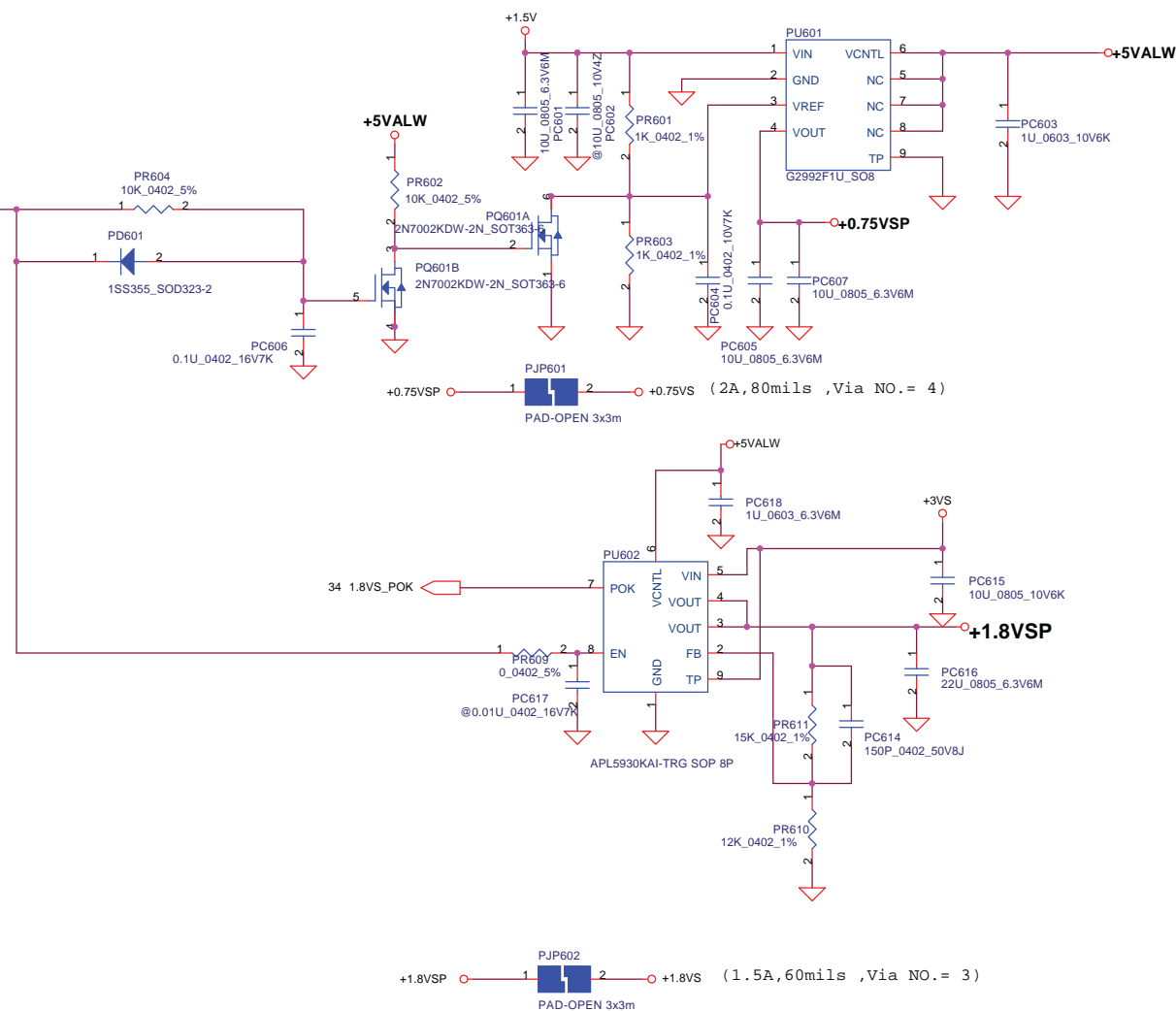
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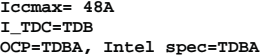
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35,38,40 SLP\_S3#



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# Version Change List ( P. I. R. List ) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21	MXM PEG Bus	01/19	Compal	Can't detect GPU of MXM board	Need reverse TX & RX bus of PEG.	0.2
2	21	MXM LVDS Bus	01/19	Compal	No display of LVDS panel	Need reverse LVDS low&high bit BUS.	0.2
3	13	RTC	01/19	Compal	RTC no function	Reverse signals of RTC connector.	0.2
4	29	JVGAFFC1	01/20	Compal	JVGAFFC1 pin23&24 was dummy, USB cacn't work	Connect JVGAFFC1 pin23&24 to SLP_S4.	0.2
5	20	DISP_OFF#	02/02	Compal	Use wrong power rail for this signal.	Currently panel spec is +3VS.	0.2
6	20	Left USB port	02/02	Compal	It's wrong port for debug	Change connection from port0 to port1 for debug.	0.2
7	21	PWR_LEVEL	02/04	Compal	Need isolation circit per HP request.	Add Q69, Q70, R397, R388, R118.	0.2
8	4	CPU FAN CONN	02/06	Compal	No GND pin of FAN connector.	Change Connector to 4 pin with GND pin.	0.2
9	4,13,24	SM BUS	02/06	HP	HP request to remove SM bus to XDP, JTAG & WLAN	Leave TP and remove signals.	0.2
10	22	Intel LAN	02/06	HP	Intel change design to remove some caps.	Remove these caps as Intel CRB design.	0.2
11	11	DDR M2 support	02/08	Compal	Data & CLK signals are reverse of U36.	Reverse CLK & DATA.	0.2
12	30	LED CTL circuit	02/06	HP	HP request to update LED control circuit.	No install R734 & R735.	0.2
13	15	Duplicate	02/06	HP	Remove R247 because of R541existing.	Remove R247.	0.2
14	13	PCH_JTAG_RST#	02/06	HP	Change R720 to NO INSTALL.	No install R720.	0.2
15	13	GPIO	02/06	HP	Change GPIO43_R to USB_OC#4 & reserve 33 ohm serial.	Add R134 but no install.	0.2
16	13	LED control	02/06	HP	Remove GND & change connection of R176.	Change R176 to 1K with install it.	0.2
17	14	CLKREQ_EXP#	02/06	HP	Change R687 PU for CLKREQ_EXP# to INSTALL.	Install R687.	0.2
18	17	PCH Power Rail	02/06	HP	Some power rail of PCH are no use.	Remove these power and add TP.	0.2
19	32	Card Reader	02/06	HP	It will need find tune value of R731 & C661.	Change R731 to 100K & C661 to 1uF X5R as Cartier first.	0.2
20	9	Debug port	02/10	HP	HP request to add debug port for IAMT.	Add JIAMT1.	0.2
21	16	WWAN CONN	02/10	HP	WOW# to WWAN connector is no longer supported.	Remove R117 and signal.	0.2
22	13	SATA port	02/10	HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 -->2.	0.2
23	31	KBC1091	02/10	HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.2
24	24	WLAN	02/10	HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.2
25	24	USB port6	02/10	HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.2
26	20	WLAN	02/10	HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.2
27	22	Intel 82578	02/10	HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.2
28	4, 16	Intel Change	02/10	HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.2
29	31	System ID control	02/17	HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.2
30	20	Webcam	02/17	HP	WEBCAM_OFF is active high, so need change design.	Add R287 to turn on Gate.	0.2
31	15	PWR_GD	02/17	HP	HP request to change design.	Add R399 and install R237.	0.2
32	15	NAND Flash	02/17	HP	HP request to change design.	Add NAND_DETECT# form U4.Y7 to JNAND1.17.	0.2
33	4	XDP PU	02/17	HP	HP request to change design.	Del R37, R38, R39.	0.2
34	22	LAN Power	02/17	HP	Remove power switch from 3V to 1V and related parts.	Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402.	0.2
35	29	Docking	02/17	HP	HP agree to remove caps for DP from MB to DOCKING.	Remove C496 ~ C511 from MB.	0.2
36	33	Super I/O	02/17	Compal	Common design change to SMSC		0.2

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# Version Change List ( P. I. R. List ) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	ESD DIODE	04/23	Compal	Wrong connection of D53 & D54, system can't boot.	Swap +5VS & GND of D53 & D54 pin 2 & 5.	0.3
2	29	SATA Port 5	04/23	Compal	It have wrong connection of JDOCK1 pin108 & pin109.	Swap SATA_PTX_C_DRX_P5/N5 of connector side.	0.3
3	28	SPI_CS0#	04/23	HP	HP request to add pull up resistor close to SPI ROM.	Reserve R6 close to U19.	0.3
4	14	SM BUS	04/23	HP	Intel request to change PU to 2.2K.	Change R199, R200 from 4.7K to 2.2K	0.3
5	23	LAN Transfermer	04/23	HP	Intel request to add 1uF cap between TRM caps to GND.	Add C264 to GND.	0.3
6	13	JTAG Port	04/24	HP	HP review need swap JTAG1 pin4 & pin6.	Swap XDP_FN16 & XDP_FN17 at JTAG1 side.	0.3
7	17	PCH +1.05VS	04/25	HP	HP review will no need connect resistor between them.	Remove R310.	0.3
8	14	PCH 25MHz Crystall	04/25	HP	No need 25MHz for PCH as common design.	No install R229, C281, C282, Y4 but add R52.	0.3
9	31	KBC1098 VCC0	04/25	HP	The VCC0 will never connect to GND.	Remove R587 from schematic.	0.3
10	16	LAN_DIS#	04/25	HP	GPIO12 of PCH have internal PU.	No install R279 and reserve R53 PD.	0.3
11	21	DPA AUX	04/25	HP	Need 0.1uF cap for Q20, Q67 gate pin.	Add C265.	0.3
12	30	WWAN_DET#	04/25	HP	Design Change PCH GPIO22 to WWAN_DET#.	Change GPIO of PCH to WWAN_DET#.	0.3
13	16	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Modify WEBCAM_OFF to WEBCAM_ON, add R66 PU for GPIO47.	0.3
14	20	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Del R350.	0.3
15	13	DOCK LED	04/25	HP	Need inverter for docking power LED signal.	Add Q71 & R67.	0.3
16	33	SER_SHD	04/25	HP	HP request to remove SER_SHD from SIO to docking.	Disconnect SER_SHD at docking side, add R7 PU to +3VS.	0.3
17	9, 10	DDR3 M1 & M3	04/30	HP	Need implement M1, M3 but reserve M2 for SI1.	Remove R91, R682~R684 and add divider for V_DDR_CPU_REF0/1.	0.3
18	17	PCH Power Rail		HP	Some power rail of PCH are no use.	Remove these power and add TP.	0.3
19	32	Card Reader		HP	It will need find tune value of R731 & C661.	Change R731 to 100K & C661 to 1uF X5R as Cartier first.	0.3
20	9	Debug port		HP	HP request to add debug port for IAMT.	Add JIAMT1.	0.3
21	16	WWAN CONN		HP	WOW# to WWAN connector is no longer supported.	Remove R117 and signal.	0.3
22	13	SATA port		HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 --> 2.	0.3
23	31	KBC1091		HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.3
24	24	WLAN		HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.3
25	24	USB port6		HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.3
26	20	WLAN		HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.3
27	22	Intel 82578		HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.3
28	4, 16	Intel Change		HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.3
29	31	System ID control		HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.3
30	20	Webcam		HP	WEBCAM_OFF is active high, so need change design.	Add R287 to turn on Gate.	0.3
31	15	PWR_GD		HP	HP request to change design.	Add R399 and install R237.	0.3
32	15	NAND Flash		HP	HP request to change design.	Add NAND_DETECT# form U4.Y7 to JNAND1.17.	0.3
33	4	XDP PU		HP	HP request to change design.	Del R37, R38, R39.	0.3
34	22	LAN Power		HP	Remove power switch from 3V to 1V and related parts.	Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402.	
35	29	Docking		HP	HP agree to remove caps for DP from MB to DOCKING.	Remove C496 ~ C511 from MB.	
36	33	Super I/O		Compal	Common design change to SMSC		
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# Version Change List ( P. I. R. List ) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	4	FAN CTRL Circuit	07/2	HP	FAN always 100% turn after power on	Del D29 & NI R133 to prevent this issue.	0.4
2	29	SATA Port 5	04/23	Compal	It have wrong connection of JDCK1 pin108 & pin109.	Swap SATA_PTX_C_DRX_P5/N5 of connector side.	0.3
3	28	SPI_CS0#	04/23	HP	HP request to add pull up resistor close to SPI ROM.	Reserve R6 close to U19.	0.3
4	14	SM BUS	04/23	HP	Intel request to change PU to 2.2K.	Change R199, R200 from 4.7K to 2.2K	0.3
5	23	LAN Transfermer	04/23	HP	Intel request to add 1uF cap between TRM caps to GND.	Add C264 to GND.	0.3
6	13	JTAG Port	04/24	HP	HP review need swap JTAG1 pin4 & pin6.	Swap XDP_FN16 & XDP_FN17 at JTAG1 side.	0.3
7	17	PCH +1.05VS	04/25	HP	HP review will no need connect resistor between them.	Remove R310.	0.3
8	14	PCH 25MHz Crystall	04/25	HP	No need 25MHz for PCH as common design.	No install R229, C281, C282, Y4 but add R52.	0.3
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13	16	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Modify WEBCAM_OFF to WEBCAM_ON, add R66 PU for GPIO47.	0.3
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16	33	SER_SHD	04/25	HP	HP request to remove SER_SHD from SIO to docking.	Disconnect SER_SHD at docking side, add R7 PU to +3VS.	0.3
17	9, 10	DDR3 M1 & M3	04/30	HP	Need implement M1, M3 but reserve M2 for SI1.	Remove R91, R682~R684 and add divider for V_DDR_CPU_REF0/1.	0.3
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22	13	SATA port		HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 --> 2.	0.3
23	31	KBC1091		HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.3
24	24	WLAN		HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.3
25	24	USB port6		HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.3
26	20	WLAN		HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.3
27	22	Intel 82578		HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.3
28	4, 16	Intel Change		HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.3
29	31	System ID control		HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.3
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